LOW-VOLTAGE LOW-POWER ANALOG-TO-DIGITAL CONVERTERS

TAO YONGHONG

(*Bachelor of Engineering, Northern Jiaotong University, China;*

Master of Science, National University of Singapore, Singapore)

A THESIS SUBMITTED FOR

THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2011

Acknowledgements

To pursue a PhD degree in part time is a challenge. It is a long journey full of pain, sadness, confusion, changes, adjustments, pleasure and fun. In last 5 years, I got a lot of help from my advisors, family, colleagues, friends and classmates. It is a pleasure to thank those who made this thesis possible.

First of all I would like to express my gratitude to my advisors, Prof. Yao Libin and Prof. Lian Yong. I was a digital design engineer before enrolling into this PhD program in analog circuit design. Prof. Yao provided me many critical hints and tips during my initial study. His guidance made me success in two tape-outs of Delta-Sigma modulator. With Prof. Lian's help, I changed my research topic to SAR ADC smoothly. I was impressed by his wide knowledge in different areas, such as DSP, digital IC, analog IC and biomedical electronics. He provided me a lot of valuable insights into my research work. His attitude of striving for excellence motivated me.

I got a lot of supports from my family. My wife Yanan constantly supported and encouraged me to accomplish this work. Without her help, I wouldn't have the chance to type this acknowledgement letter. I owe my deepest gratitude to my parents-in-law for taking care of my son while I was struggling for the tape-outs.

I would like to thank Ms. Kafai Leung, my supervisor in Silicon Labs, for bringing me into such a great company with so many talented engineers. Especially, I feel very lucky to get the chance to work with Dave R. Welland, the cofounder of this company, who periodically ruins my blind optimism and pushes me to dig into the details. The discussion with Shan Wang and other colleagues always sharpens my mind.

In addition, I would like to thank my friends for their support, especially, Ya Dong, Hong Sair, Jeffery, Li Yi, Qian Yue, Hu Changhui, Zhang Yayue, Zheng hui, Zhang Chengjian, Li Xiaobo, Qi Xiaofei and Shen Ruifen.

As a part time student, I seldom meet my classmates in school. However, they offered me all kinds of help. Especially, I am indebted to Jinghua, Zhenglin, Wang Lei and xiaoyang for their selfless help.

Finally, I dedicate this thesis to my parents.

Singapore 2011 Tony, Tao Yonghong

Table of Contents

Summary

Low voltage, low power analog-to-digital converters (ADC) are required in many applications. This work covers two popular ADC designs: Delta-Sigma modulator and Successive-approximation (SAR) ADC.

The high-speed Delta-Sigma modulator is targeted to the digital communication system, especially digital subscriber line (DSL) application, which requires an ADC with 13~14 bit resolution and a few MS/s conversion rate. The optimization at system level enables its low power consumption even under low supply voltage. Especially, the input feedforward topology relaxes the design specifications from each building block. In this thesis, two Delta-Sigma modulators based on this topology are presented. A 1.0 V, 82 dB, 2.5 MS/s modulator for ADSL system is fabricated and tested successfully. The second modulator targets to 25 MS/s conversion rate, for VDSL application. Although this design is not fabricated, its design procedures are documented in details.

The low power SAR ADC is dedicated to the portable sensing systems, which require digitizing either slowly-varying or sampled DC signals. Two chips with different approaches to low power consumption are fabricated and tested successfully. The design novelties in the first ADC include: A modified, biasing-free CMOS inverter is adopted as the key amplifier, with an adaptive digital calibration technique as assistance; this V_{cm} buffer is also reused as the pre-amplifier for the current-mode latched comparator; dual thermometer decoders are used for the split capacitor array. This 10-bit ADC achieves 1 MS/s conversion rate under 1.0 V supply voltage. The second SAR ADC features a serially connected capacitor array, which reduces its capacitive load to the amplifier and lowers the power consumption. With supply voltage of only 0.8 V, this 10-bit ADC also achieves 1 MS/s conversion rate.

List of Tables

List of Figures

List of Symbols

ADC:	Analog-to-Digital Converter
ADSL:	Asymmetric Digital Subscriber Line
BW:	Bandwidth
CMFB:	Common Mode Feedback
DAC:	Digital-to-Analog Converter
DSL:	Digital Subscriber Line
DR:	Dynamic Range
DEM:	Dynamic Element Matching
DSM:	Deep Sub-Micron
DSP:	Digital Signal Processor
DNL:	Differential Non-Linearity
ECG:	Electrocardiography
ENOB:	Effective Number of Bits
FFT:	Fast Fourier Transform
FOM:	Figure-of-Merit
INL:	Integral Non-Linearity
LSB:	Least Significant Bit
MSB:	Most Significant Bit
NTF:	Noise Transfer Function
OTA:	Operational Transconductance Amplifier
OSR:	Oversampling Ratio
SAR:	Successive Approximation Register
SC:	Switched Capacitor

SNR:	Signal-to-Noise Ratio
SNDR:	Signal-to-Noise and Distortion Ratio
STF:	Signal Transfer Function
VDSL:	Very-high-speed Digital Subscriber Line

CHAPTER 1 INTRODUCTION

1.1 Background

The world is becoming more digitized every day, because of the popularity of the digital computing and digital signal processing. The main advantage of digital circuits, over the analog counterparts, is that they are less sensitive to disturbance and more robust in supply and process variations. The implementation is much easier and more programmable. Meanwhile, the design flow can be easily automated by matured EDA tools. With advanced process technology, the performance of digital circuits is boosted. With more and more function integrated in a single chip, the manufacturing process is pushed into ultra deep sub-micron (DSM) era.

Nevertheless, the world is still analog. The signals processed by digital circuits are still from the analog world, and are sent back to the analog world after processing. Since the digital devices have to interact with the analog world, the more "the world is becoming digital," the more devices are required that interface the analog world with the world of the digital processors. One of the devices is the analog-to-digital (A/D) converter, which translates the signals from the analog format into digital one.

Figure 1.1 illustrates the modern signal processing system with analog signals as input and output. The digital signal processor (DSP) is the core of this system, due to its high dynamic range, low cost and good repeatability. However, the physical world is in "analog" style, such as voice, audio, video, temperature, pressure and so on. An analog-to-digital converter (ADC) takes the real world analog signal and transforms it into a digital data stream. This stream is processed by the DSP core, and the resulting

digital output signal is reconverted into analog form by a digital-to-analog converter (DAC).

Figure 1.1: Modern signal processing system.

The ADC can be classified into two categories: Nyquist-rate and oversampling converters. For the Nyquist-rate ADC, there exists a one-to-one correspondence between analog input and digital output. Each input sample is processed separately, regardless of previous input samples. That is to say, there is no memory effect. The analog input is represented as

$$V_{in} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + ... + b_N 2^{-N}) \quad (1.1)$$

where, V_{ref} is the reference voltage and $b_1,\ldots,b_N$ is the digital outputs. For the Nyquist-rate ADC, the lowest sampling frequency follows the Nyquist criterion and is twice the signal bandwidth. In most cases, the linearity of the Nyquist-rate ADC is determined by the matching accuracy of the analog components (resistors, current sources or capacitors) used in the implementation. For the modern CMOS technology, the achievable effective number of bits (ENOB) is about 12 without complex trimming.

Oversampling ADC is able to achieve higher accuracy, by using the sampling rates much high than the Nyquist rate. The typical oversampling ratio is between 8 and 512. This converter has memory effect, which generates each digital output based on all preceding inputs. So, there is no one-to-one correspondence between analog inputs and digital outputs. However, the accuracy requirements on the analog components are much relaxed compared with those in Nyquist-rate converters. The cost paid for

high accuracy thus includes faster operation and extra digital filters for post-processing.

Because of different paid cost and achievable accuracy, the adoption of Nyquist-rate or oversampling ADC is based on its application context.

1.2 Motivation

The trend in integrated circuit fabrication is mainly driven by the digital circuit designs. It has been on a move toward decreased geometry sizes to increase circuit capacity and speed. As transistor sizes decrease, the circuit functionality of a given area of substrate can be increased. Smaller device sizes also yield lower parasitic capacitance which increases speed and decreases power consumption. As process geometries decrease, operating voltages must be scaled down due to increased electric fields and reduced breakdown voltages caused by higher doping profiles.

Another trend is to integrate more and more analog functions with digital circuits. The advantage is the resulting compact and low-cost single chip solution. With integration, the interface between analog and digital becomes easier and the PCB area can be reduced. To integrate with digital circuits and fabricate with advanced process, the supply voltage of analog circuits has to reduce. Low voltage analog-to-digital converter has become a necessity.

Low power consumption is critical for modern applications. Consumers of portable electronics demand smaller devices with longer battery life. Lower power consumption brings higher competence in a rapidly changing market. Even for the communication equipments, lower power dissipation produces less heat, saves circuit board space and cost. The power consumption of ADCs becomes a important criteria for performance comparison. Figure 1.2 provides a complete ADC survey [1] based on power efficiency. The trend for lower power consumption is obvious.

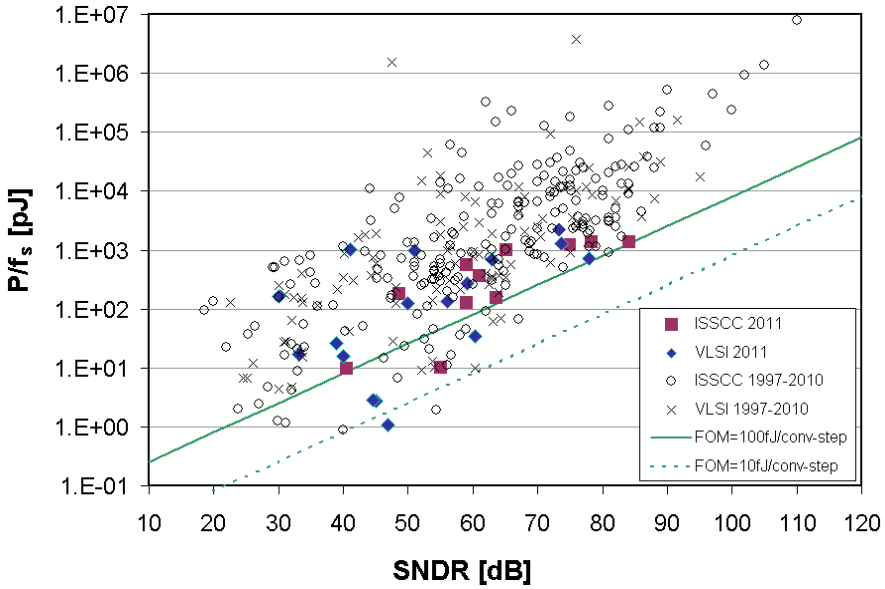

Figure 1.2: ADC survey for power consumption.

This research work covers both oversampling and Nyquist-rate ADCs. The study on low voltage, low power and high speed Delta-Sigma modulator targets for digital communication systems, especially digital subscriber line (DSL) application. With supply voltage of 1.0 V, the achieved conversion rate is 2.5 MS/s for ADSL standard and 25 MS/s for VDSL, with the dynamic range of 80 dB.

For the Nyquist-rate ADC, the successive-approximation register (SAR) A/D converter is explored, for the application of portable sensing systems. With the supply voltage around 1.0 V, the 10-bit SAR ADCs achieve the conversion rate of 1 MS/s.

1.3 Thesis Organization

The thesis covers the design of both Delta-Sigma modulator and SAR ADC. Chapter 2 is the literature review for both ADC architectures. The basic operation theory, important concepts and current researching status are discussed.

Chapter 3 presents the design of a single-bit Delta-Sigma modulator. It achieves conversion rate of 2.5 MS/s and dynamic range of 82 dB, under the supply voltage of 1.0 V. The experimental results are provided to validate the modulator architecture.

Chapter 4 illustrates the architecture design of a multi-bit Delta-Sigma modulator. The targeted conversion rate is 25 MS/s with dynamic range of 85 dB and supply voltage of 1.0 V. Although the experimental results are not provided, the detailed design procedures are provided for future research work.

Chapter 5 describes the design of a low power 10-bit SAR ADC for sensing systems. The supply voltage is 1.0 V and conversion rate is 1 MS/s. With total power consumption of 18 uW, the achieved Figure-of-Merit (FOM) is 35 fJ/conversion.

Chapter 6 covers the design of another low power 10-bit SAR ADC for sensing systems. The conversion rate is 1 MS/s while the supply voltage is reduced to 0.8 V and the power consumption decreases to 9 uW. The achieved Figure-of-Merit (FOM) is 20 fJ/conversion.

Chapter 7 concludes the whole thesis and provides some discussion for future research work.

1.4 List of Publication

1.4.1 Low Voltage Delta-Sigma Modulator

Y. Tao and L. Yao, “A 1-V, 81-dB, 780-KS/s, Sigma-Delta Modulator in 0.13-μm Digital CMOS Technology,” IEEE International Conference on Electron Devices and Solid-State Circuit 2008 (EDSSC), Hong Kong, China, Dec 2008. [Best Paper Award]

Y. Tao, L. Yao and Y. Lian, “A 1-V, 82-dB, 2.5-MS/s, single loop, single bit delta-sigma modulator in 0.13-μm CMOS technology,” Journal of Analog Integrated Circuits and Signal Processing, Aug. 2011.

1.4.2 Low Voltage SAR ADC

Y. Tao and Y. Lian, “A 1 V, 1 MS/s, biasing-free, 10-bit SAR ADC for Sensing Systems,” preparation for IEEE Transactions on Circuits and Systems I.

Y. Tao and Y. Lian, “A 0.8 V, 1 MS/s, 10-bit SAR ADC for Sensing System,” preparation for IEEE Journal of Solid-State Circuits.

CHAPTER 2 LITERATURE REVIEW

2.1 Introduction

2.1.1 Building Blocks in Analog-to-digital Converters

The basic operation of an analog-to-digital converter (ADC) can be split into a sequence of simple elementary steps. Figure 2.1 represents an A/D converter as the cascade of four functions: continuous-time anti-aliasing filtering, sampling, quantization and data coding.

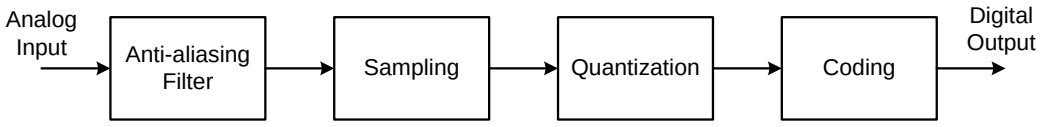

Figure 2.1: The steps of an analog-to-digital converter.

The anti-aliasing filter protects the information content of the signal. Use an anti-aliasing filter in front of every quantizer to reject unwanted interferences outside of the band of interest. A sampler transforms a continuous-time signal into its sampled-data equivalent. Amplitude quantization changes a sampled-data signal from continuous-level to discrete-level. The dynamic range of the quantizer is divided into a number of equal quantization intervals, each of which is represented by a given analog amplitude. The quantizer modifies the input amplitude into a value that represents which quantization interval it resides in. The quantization error is an unavoidable fundamental limit of the quantization process: it becomes zero only when the number of bits goes to infinity, which is unfeasible in practice. The quantization error can be treated as quantization noise while the input signals have large busy

amplitudes. Coding the quantized amplitude is the last function of an A/D converter. Binary representation is an effective coding scheme.

2.1.2 ADC Architectures

There are many types of ADC architectures which are suitable for different targeted applications. The ADC architectures are normally classified as following:

- Slope Converters
- Successive approximation
- Flash
- Folding
- Time-interleaved / parallel converter
- Residue type ADCs
    - Two-step
    - Pipeline
    - Algorithmic
- Oversampled ADCs

In this work, two kinds of widely used ADCs are explored: Delta-Sigma modulator (belong to oversampled ADC) and successive approximation (SAR) ADC. In the literature review, some key concepts are discussed after introducing the basic operation theory, for both architectures. To get some ideas of the state-of-the-art, the literature review is performed for both ADCs.

2.2 Delta-Sigma Modulator

2.2.1 Oversampling and Delta Modulation

In signal processing, oversampling is the process of sampling a signal with a sampling frequency significantly higher than twice of signal bandwidth. It can reduce the design difficulty of analog anti-aliasing filter by enlarging its transition band. It can also improve the resolution of Nyquist ADC by adding some dithering noise. For fast varying inputs, the quantization noise can be reduced by using oversampling and additional digital filter. Oversampling spreads the quantization noise power over the frequency band from DC to $f_s/2$, where f_s is the sampling frequency. Digital filter can attenuate the quantization noise above the signal bandwidth.

Delta modulator and Delta-Sigma modulator are two main types of oversampling converters. The Delta-Sigma modulator is developed from Delta modulator [2]. The basic building block of Delta modulator is shown in Figure 2.2. It is a feedback loop, containing an internal low resolution ADC and DAC, as well as an integrator. The idea of Delta modulator is converting the changes of input signal into digital formats. At the receiver side, another integrator is required to recover the original signal. However, this modulator is prone to additive noise in the communication channel because of the integration at the receiver side.

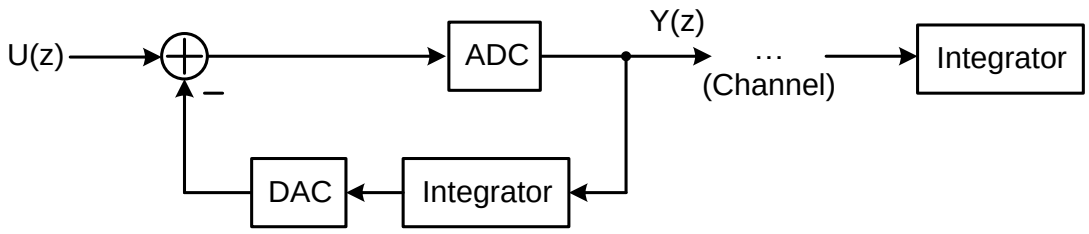

Figure 2.2: The Delta Modulator.

The total transfer function of Delta modulation system is unchanged by moving the location of integrator at receiver side, as shown in Figure 2.3. This avoids the

accumulation of channel noise. However, the integrator at input side may overflow. To solve the new issue, both integrators at input and feedback paths are moved into the loop. The developed system is Delta-Sigma modulator shown in Figure 2.4. The understanding of this development procedure is useful during architecture design.

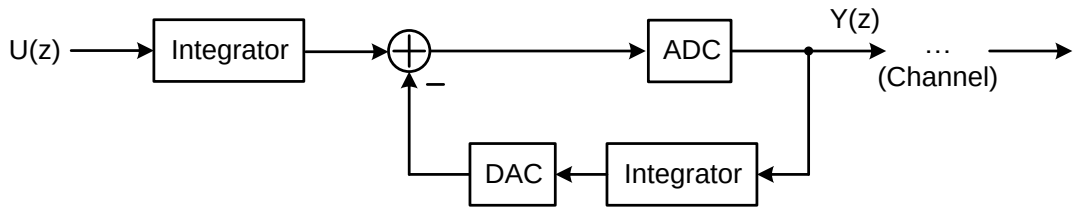

Figure 2.3: The development of Delta-Sigma modulator.

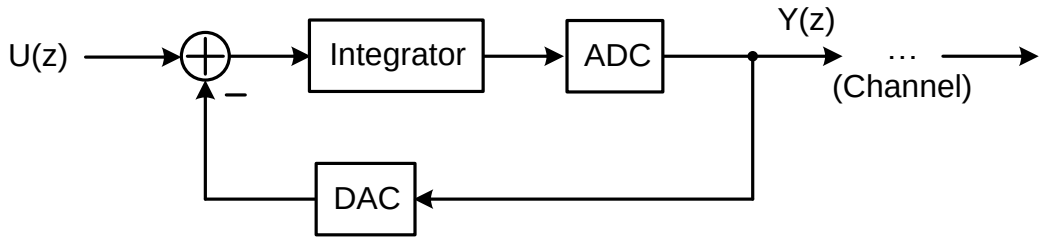

Figure 2.4: The topology of Delta-Sigma modulator.

2.2.2 Noise Shaping

The Delta-Sigma modulation is derived from Delta modulation. The first order delta-sigma modulator is shown in Figure 2.5.

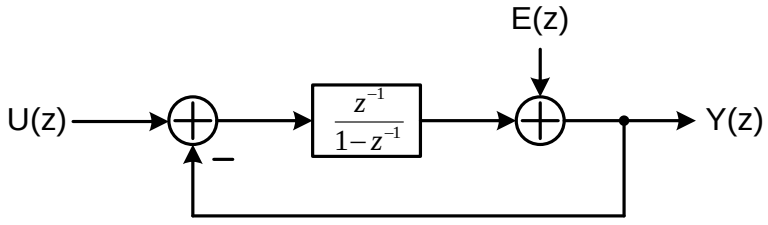

Figure 2.5: Linear model for first order Delta-Sigma modulator.

Y(z) can be calculated easily by

$$Y(z) = U(z)z^{-1} + (1 - z^{-1})E(z), \qquad (2.1)$$

where, *E(z)* is the additive quantization noise and is first-order differentiated. That is to say, the quantization noise is attenuated at low frequency and expanded at high frequency. This process is commonly named as *noise shaping*. Combined with oversampling technique, the quantization noise in the signal band is further attenuated. The function of noise shaping can be calculated as

$$S_q(f) = (2\sin(\pi f T))^2 S_e(f), \qquad (2.2)$$

where, f is the frequency variable, $T = 1/f_s$ is the sampling period, $S_e(f)$ is the 1-side PSD of the quantization noise of internal ADC. For fast varying input signals, the noise spectrum is

$$S_e(f) = \frac{\Delta^2}{6 f_s}, \qquad (2.3)$$

where, Δ is step size of the internal ADC. The NTF of first order modulator is plotted in Figure 2.6.

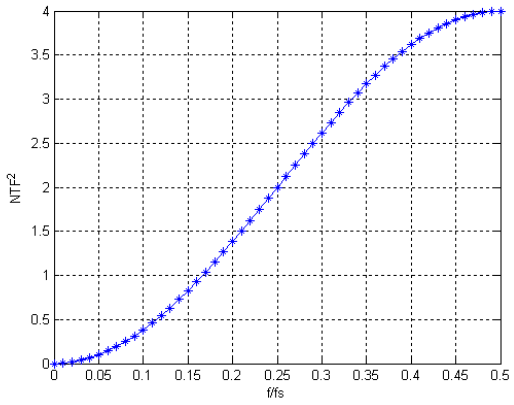

Figure 2.6: Noise shaping function for first-order modulator.

Integrating $S_q(f)$ between 0 and f_B (signal bandwidth) gives the in-band noise power

$$q_{rms}^{\ 2} = \frac{\pi^2 \Delta^2}{36 * OSR^3}, \qquad (2.4)$$

where, *OSR* defined as $f_s/(2*f_B)$. The loop filter can be extended to higher order easily, with L as the order of loop filter

$$q_{rms}^{\ 2} = \frac{\pi^{2L}\Delta^2}{12*(2L+1)*OSR^{2L+1}}. \qquad (2.5)$$

The ideally achievable SNR with different *OSR* and L is shown in Figure 2.7. For the 2nd-order modulator, the ENOB is increased by 2.5 bits while doubling the *OSR*, compared with 1.5 bits for 1st-order one.

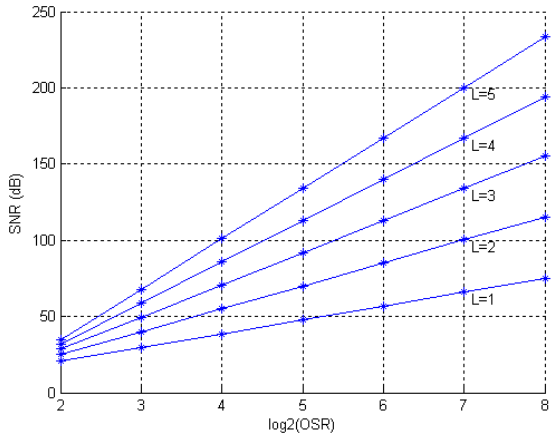

Figure 2.7: The SNR vs. OSR for Delta-Sigma modulator.

However, with high order loop filter, it becomes more difficult to maintain the stability. The internal ADC is normally overloaded, which reduces the achievable SNR.

2.2.3 Multi-stage (MASH) Modulator and Multi-bit Modulator

To ease the stability problems associated with the high-order loop filter, the modulators with low-order filter are cascaded to achieve the same performance. The basic concept is shown in Figure 2.8.

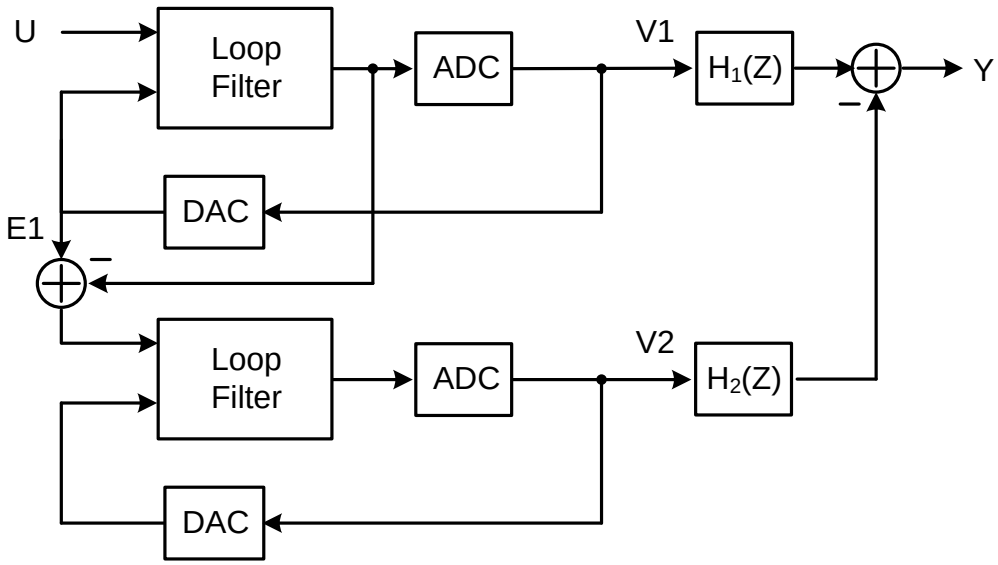

Figure 2.8: A multi-stage Delta-Sigma modulator.

The quantization noise from first loop filter E_1 is feed to the input of 2nd loop filter. The digital filter stages H_1 and H_2 are designed such that in the overall output Y the first stage quantization error E_1 is cancelled. With this arrangement, the order of overall noise shaping is the sum of the order from both loop filters. However, the stability behavior is that of a low order loop filter.

However, if the quantization noise from first stage is not fully cancelled out due to the imperfections of analog building blocks, the overall noise shaping will be degraded. High DC gain from the building OTA is the usual requirement.

For the Delta-Sigma modulator, the overall accuracy is limited by the linearity of feedback DAC. This occurs because the in-band part of the DAC output signal is forced by the feedback loop to follow the input signal very accurately. Hence, if the DAC is nonlinear, its digital input must be distorted to give an accurate analog output. The single-bit DAC is inherently linear because there are only two output levels. It is widely used for the early Delta-Sigma modulators. However, the single-bit ADC has ill-defined gain factor and the loop must be stable over a wide range of loop gains. This reduces the allowable input signal swing, and hence the achievable SNR.

For a multi-bit quantizer, the loop is inherently more stable since the quantizer gain is well-defined, and the no-overload range of the quantizer is increased. Meanwhile, the quantization noise decreases by 6 dB for each additional bit added to the quantizer. Even with low OSR value, it is possible to achieve high SNR. The linearity of multi-bit feedback DAC can be improved by manipulating the elements of the DAC dynamically. This reduces the in-band portion of the error signal introduced by DAC nonlinearity and is named as mismatch shaping. Its effectiveness increases with increasing OSR.

2.3 Key Concepts for Delta-Sigma Modulator

2.3.1 Linear Model of Single-bit Quantizer

For a single-bit quantizer, there is only one threshold. The digital output is just the sign bit of the analog input, so the gain of single-bit quantizer is not easily defined. To get the linear model, the gain can be obtained in a statistical way. Assuming *y* is the input and *v* is the digital output, the quantization error e is

$$e = v - ky, \tag{2.6}$$

where, *k* is the quantizer gain. The optimal value of *k* can be derived by minimizing the mean square error of *e* [3], which is defined as

$$\sigma_e^{\,2} = \lim_{N\to\infty} \frac{1}{N} \sum_{n=0}^{N} e(n)^2 = < e,e > , \tag{2.7}$$

where, <*e*,*e*> is the scalar product. The mean square error can be calculated as a function of *k* as

$$\begin{aligned} &< e,e > = < v - ky, v - ky > \\ &= < v,v > -2k < v,y > + k^2 < y,y > \end{aligned} . \tag{2.8}$$

The mean square is minimized for

$$k = \frac{< v, y >}{< y, y >}. \qquad (2.9)$$

Clearly, the optimal value of k for the linear model of single-bit quantizer is dependent on the statistics of input y. For the single-bit Delta-Sigma modulator, it can be found from extensive numerical simulation.

2.3.2 Idle Tones in Delta-Sigma Modulator

First, consider a first-order modulator with DC input. The modulator input is u and output is v, with y as the quantizer input. Assuming u = 1/2 and $y(0)$ = 1/2, then the modulator output is described in Table 2.1.

Table 2.1: The Delta-Sigma Modulator shows idle tones.

n	0	1	2	3	4	5
y(n)	1/2	0	-1/2	1	1/2	0
v(n)	1	1	-1	1	1	1

Hence, the output is periodic with a period of 4, which indicates the tone at $f_s/4$ (f_s is the sampling frequency). With high enough OSR, this tone is out of signal bandwidth. This observation can be extended to all other rational DC input. This periodic sequences generated by rational DC input are named as idle tone (or limit cycles, pattern noise).

With low DC inputs, such as u = 1/100, the generated tone is located as $f_s/200$ and its harmonics, which is within the signal bandwidth with OSR = 128. Both the frequency and power of the tones are functions of the DC input. In some applications, such as in digital audio, idle tones cannot be tolerated, since the human hearing apparatus can detect the tones even 20 dB below the level of any white noise present. The idle tones can be prevented by using higher-order loop filter or dithering.

2.3.3 Stability of First-order and Second-order Modulator

Linear analysis based on Bode plots would predict unconditional stability for first-order modulator, since the loop gain decreases by -20 dB/decade and the loop phase is -90 degree at all frequencies. However, this prediction does not take into account the nonlinear behavior inside the modulator loop. Assume u is the modulator input and y is the quantizer input. If $|u| > 1$, y will become unbounded. Vice verse, if $|u| \leq 1$ and the initial value of y satisfies $|y(0)| \leq 2$, then the loop will remain stable, with $|y|$ bounded by 2. This stability condition is enough even for the time-varying u. If $|y(0)| > 2$ and $|u| \leq 1$, then the modulator output will contain a string of 1 or -1 until previous condition is satisfied.

In conclusion, the stability requirement for first-order Delta-Sigma modulator is $|u| \leq 1$, where 1 is the normalized feedback reference voltage.

One exampled second-order modulator is shown in Figure 2.9.

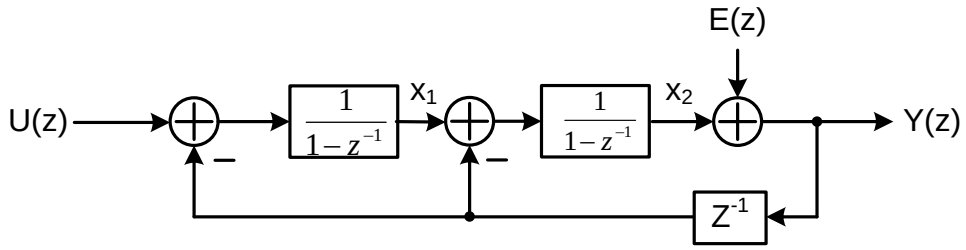

Figure 2.9: A second-order Delta-Sigma modulator.

Assume u is the input, x_1 and x_2 are the integrator outputs. With dc inputs satisfying $|u| < 1$ the following bounds apply [4]:

$$|x_1| \leq |u| + 2,$$
$$|x_2| \leq \frac{(5-|u|)^2}{8(1-|u|)}. \qquad (2.10)$$

The internal states of 2nd-order modulator are guaranteed to be bounded for inputs less than 1 in amplitude, although the bound on x_2 does become arbitrarily large as $|u| \rightarrow$

1. It is wise to limit the modulator input to $|u| < 0.8$ or 0.9, to prevent large x_2. Unfortunately, even though such an input limit will keep the modulator state reasonable for dc and slowly-varying inputs, it is possible for the modulator state to become much larger than intended. It is therefore important to include means for detecting overly large states and placing the modulator in a "good" state.

2.3.4 Stability of High-order Delta-Sigma Modulator

High-order Delta-Sigma modulator is found to offer improved performance at the expense of more hardware and reduced signal range. The range of input magnitudes over which the modulator functions properly is called the stable input range. In a high-order modulator, especially in one employing single-bit quantizer, the stable input range is usually a few dB below the full-scale range of the feedback DAC. This loss in range usually results from the nonlinear effects of quantizer overload rather than from insufficient linear range in the filter.

For single-bit modulator, the most widely-used approximation criterion is the (modified) Lee criterion [5]. It states a binary Delta-Sigma modulator with an NTF = $H(z)$ is likely to be stable if $\max|H(e^{jw})| < 1.5$. Note that this criterion is neither necessary, nor sufficient. Nevertheless, due to its simplicity, it is of some use. For moderate-order modulators (order 3 or 4), slightly higher value can be used for $\max|H(e^{jw})|$.

One important note to Lee's rule is that it has no solid theoretical foundations, and needs to be confirmed by extensive simulations. Another approach for stability check is the linear model shown in Figure 2.10.

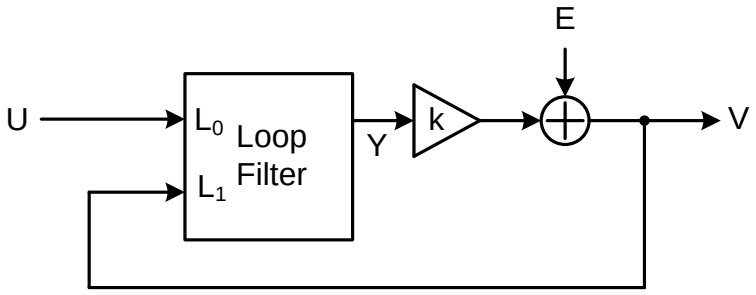

Figure 2.10: Linear model for higher-order modulator.

Here, the quantization has been replaced by a multiplication with a constant k and by the addition of the random noise E. The constant k is defined as (v is sign of y)

$$k = \frac{< v, y >}{< y, y >} = \frac{E[|y|]}{E[y^2]}. \qquad (2.11)$$

Then the effective NTF can be written as

$$NTF_k(z) = \frac{1}{1 - kL_1(z)} = \frac{NTF_1(z)}{k + (1-k)NTF_1(z)}, \qquad (2.12)$$

where, $NTF_1(z)$ is the NTF with $k = 1$. By drawing the root-locus plot with $0 < k < 1$, the stability may be predicted [6].

Unfortunately, since a Delta-Sigma modulator is a non-linear system, the quantizer gain is signal-dependent and this dependency can't be captured by any linear model. In practice, the designer of high-order single-bit modulator must resort to extensive simulations. Worst-case input signal should be applied. As R. Adams suggests [7], a representative worst-case signal is a square wave with largest permissible amplitude and with a fundamental frequency ω_f equal to that of the dominant (high-Q) pole of the NTF.

For the multi-bit modulators, there is a useful theoretical result. Assume a modulator with M-step (or M+1 level) quantizer. Let the initial $y(0)$ to the quantizer to be within its linear (no overload) range. Then the modulator is guaranteed not to experience overload for any input $u(n)$ such that $\max|u(n)| \leq M + 2 - \|h\|_1$, where $\|h\|_1$ is sum of all

|*h*(*n*)|. The *h*(*n*) is the inverse z-transform of the NTF *H*(*z*). Compared with the single-bit modulator, the stability issue from multi-bit one is more relaxed.

2.4 Circuit Considerations for Delta-Sigma Modulator

Switched-capacitor integrator, shown in Figure 2.11, is widely used in discrete-time Delta-Sigma modulator.

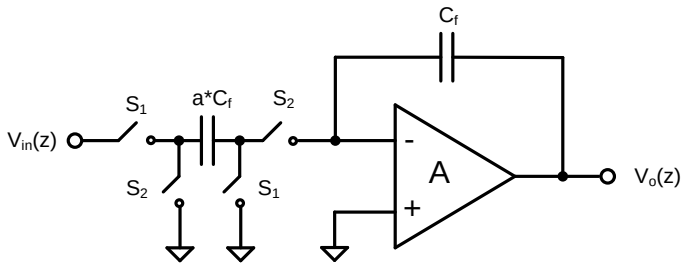

Figure 2.11: Switched-capacitor integrator.

With infinite DC gain from OTA, the difference equation from time domain is

$$V_o(z) = V_o(z) * z^{-1} + a * V_{in}(z) * z^{-1}. \quad (2.13)$$

With finite DC gain from OTA, the effective gain from the integrator can be calculated as

$$V_o(z) = \frac{A}{1+a+A}\{(\frac{1}{A}+1)V_o(z) + aV_{in}(z)\}z^{-1}. \quad (2.14)$$

This equation can be used to model the finite gain effect during MATLAB transient simulation.

For high speed Delta-Sigma modulator, the kT/C noise is a critical factor during the circuit implementation, compared with flicker noise. The kT/C noise is derived from the simple circuit in Figure 2.12.

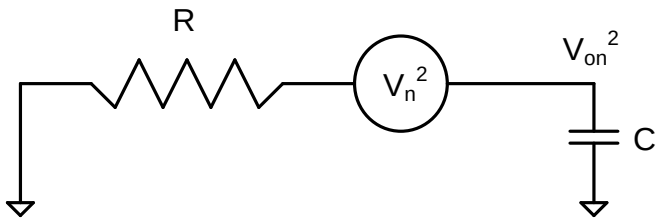

Figure 2.12: Circuit for kT/C noise calculation.

The noise voltage spectral density generated from a resistor is $4kTR$ V^2/Hz. The total noise power can be found from the integral

$$e_T^{\,2} = \int_0^{\infty} \frac{4kTR}{1+(2\pi fC)^2}\,df = \frac{kT}{C}. \qquad (2.15)$$

For the switched-capacitor integrator, the kT/C noise from first integrator is most critical. This will decide the minimum size of first input capacitor.

For the discrete-time Delta-Sigma modulation, the variation of filter coefficients is determined by the capacitor mismatch. The mismatch between any two capacitors is expressed as a deviation of the measured device ratio from the intended device ratio. This mismatch can be caused by some random statistical fluctuations, which can be categorized into peripheral fluctuations and areal fluctuations. The standard derivation can be expressed as

$$S_c = \frac{1}{C^{0.5}}\left(k_a + \frac{k_p}{C^{0.5}}\right), \qquad (2.16)$$

where, k_p is the coefficient for peripheral fluctuations and k_a for areal fluctuations. For large capacitor, areal term dominates and the random mismatch becomes inversely proportional to the square root of capacitance.

This mismatch between capacitors slightly changes the effective gain from switched-capacitor integrator. This must be taken into consideration during capacitor sizing.

For the OTA used in switched-capacitor integrator, the output swing is an important specification. However, the DC gain is not flat within the valid output range, which is

shown in Figure 2.13. This nonlinearity can be modeled in MATLAB during behavioral simulation.

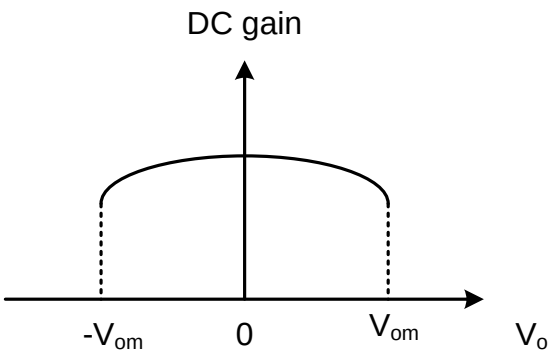

Figure 2.13: The DC gain nonlinearity from OTA.

2.5 Delta-Sigma Modulator in Literature

The proliferation of broadband communications systems is stimulating the demand for high-resolution (13~14-bits) analog-to-digital (A/D) converters with signal bandwidths on the order of 1 MHz or more. To get an overview of the research status in high-speed Delta-Sigma modulator, the literature review is performed within the papers from JSSC and ISSCC published from 2004 to 2008. (Please note I changed my research topic to SAR ADC in 2009.) It is summarized in Table 2.2.

Table 2.2: Literature searching for high-speed Delta-Sigma modulators.

Index	Supply voltage (V)	Sampling Frequency (MHz)	Conv. Rate (Ms/s)	Dynamic Range (dB)	Power Cons. (mW)	Year of Publish
[8]	1.8	200	25	84	200	2004, JSSC
[9]	1.8	32	4	83	149	2004, JSSC
[10]	1.5	105	2.2	82	7	2004, ISSCC
[11]	1.2	40	2.5	96	87	2005, JSSC
[12]	---	20	2.5	100	475	2006, ISSCC
[13]	3.3	80	20	75	240	2006, ISSCC
[14]	1.8	144	4.4	86	13.8	2006, ISSCC
[15]	1.8	100	8	73	35	2006, ISSCC
[16]	2.4	125	2.5	84	14	2007, JSSC
[17]	1.5	100	8.4	81	28	2008, JSSC

In [8], one high speed delta sigma modulator with conversion of 25 MS/s is implemented. With the supply voltage of 1.8V, the modulator runs at the sampling frequency of 200MHz. This delta sigma modulator has high sampling frequency and conversion rate, while achieving the resolution of 14-bit. The modulator is built with a discrete time, 5^{th}-order, feed-forward, single loop architecture. With gain boosting technique, the OTA gain is up to 90dB, which is favorable to suppress the gain non-linearity in feed-forward topology. With the switched capacitor passive summation circuitry, one additional amplifier is inserted between the loop filter and quantizer.

The main drawback of this design is its high power consumption. It is mainly due to the power hungry gain boosted OTA and quantizer pre-amplifier.

In [9], a delta sigma modulator with 14-bit resolution and 4 MS/s conversion rate is presented. With the low oversampling ratio of 8, the modulator is running at the sampling frequency of 32 MHz. The main contribution of this work is to propose one new hybrid architecture, based on the established relationship between Qmax (max out-of-band quantization noise gain) and dynamic range. The proposed architecture is evolved from the normal feed-forward topology, with additional local feedback between any two neighbor integrators. Because of the architecture, the OTA gain is reduced to 43.5 dB for this single stage loop filter. The main drawback of this design is from the complexity of the loop filter. Too many local feedback loops make the implementation difficult.

In [10], a power optimized 14-bit SC delta sigma modulator for ADSL application is implemented. The main contribution of this paper is to get the conversion rate of 2.2 MS/s with the power consumption of only 7 mW. With the supply voltage of 1.5 V, only 4.67 mA is consumed for the sampling frequency of 105 MHz. For the sake of stability, a 2^{nd}-order loop filter is design. To get the 14-bit resolution, the OSR is set as 192 and 3-bit quantizer is used. The modified input feed-forward topology is used to lower the internal signal swing. In this design, the input is feed into both 2^{nd} integrator and quantizer. The main drawback of this design is to choose a 2^{nd}-order loop filter because of the stability difficulty in high-order design. This necessitates high OSR and high sampling frequency, which is not favorable for low power design. The idle tone is more visible in the output spectrum because of the low-order filter design. Another drawback is to feedback the DAC output to the inputs of both

integrators. This increases the design complexity, especially when multi-bit quantizer is utilized.

In [11], one discrete time delta sigma modulator is implemented. It achieves the conversion rate of 2.5 MS/s and dynamic range of 96 dB (15-bit resolution), with the supply voltage of only 1.2 V. The design objectives are achieved by the architecture design. Input feed-forward method is applied together with multiple-stage architecture, to get a low OSR of 16. The OTA DC gain is only 54 dB, which is benefited from the input feed-forward topology. The main contribution of this work is to design the delta sigma modulator at low supply voltage with low power consumption. However, the linearity will be degraded if the filter coefficients are not well matched between different stages in MASH architecture. The harmonics in the output spectrum may be partially due to this mismatching together with non-linearity.

In [12], one delta sigma modulator with peak SNR of 100 dB and conversion rate of 2.5 MS/s is presented. Same as [11] both input feed-forward and MASH are applied, with the OSR of 8. However, the gain-boosting technique is used. The possible reason for the higher OTA DC gain is due to the design target of 100 dBFS for the 3^{rd} order harmonics. The power consumption is fairly high - 475 mW. This is mainly because of the gain boosting in the OTA for integrator and the amplifier for reference buffer.

In [13], one high speed A/D data converter with conversion rate of 20 MS/s is designed. The main building block is the 2^{nd}-order discrete time delta sigma modulator, with 4-bit quantizer. The quantization error from the delta sigma modulator is amplified by 4X times and feed into another 9-bit pipeline ADC. The digital output from both delta sigma modulator and pipeline ADC are combined in a digital filter with LMS (least mean square) algorithm embedded. The decimation filter

is also integrated. The power consumption is 240 mW with the supply voltage of 3.3 V for analog. This work claims high SFDR of 87 dB, which is higher than that in [8].

In [14], one delta sigma modulator with conversion rate of 4.4 MS/s is implemented. With the oversampling ratio of 32.7, the achieved dynamic range is up to 86 dB. With the supply voltage of 1.8 V for analog, the power consumption is only 14 mW. A local input feed-forward technique is used around the first integrator. Another global input feed-forward is implemented in the digital manner: the input is quantized first and summed together with the modulator's main quantizer. The drawback of this design is requiring two multi-bit quantizer and three multi-bit DAC. This increases the design difficulty.

In [15], one delta sigma modulator with conversion rate 8 MS/s is designed for the digital TV receiver. With the selected OSR of 12, the sampling frequency is up to 100 MHz. However, the dynamic range is only 73 dB. Input feed-forward method is used to suppress the gain non-linearity. Meanwhile, double sampling technique is used to alleviate the timing constraints on the quantizer and DWA. A folded cascoded and current-mirror OTA is used in the SC integrators for low power consumption. The modulator consumes 34 mW power with the supply voltage of 1.8 V.

In [16], one 14-bit, discrete time delta sigma modulator with conversion rate of 2.5 MS/s is implemented. The architecture is very close to that in [8]. The main difference is to use the proposed switched-capacitor split-path pseudo-differential amplifiers. The basic idea is evolved from a telescopic OTA without tail current. The P-input device and N-input device operate in different time slot to implement negative feedback, which eliminates the requirement of input common mode voltage. With the supply voltage of 2.4 V, the modulator consumes the power of 14 mW. Both 2^{nd} and

3^{rd} harmonics are clearly visible in the output spectrum, which leads to the peak SNDR of only 73 dB.

In [17], one wide-band high linearity delta sigma ADC is described. The main contribution is to use noise coupling together with timing interleaving. The noise coupling is built between two similar low-order delta sigma modulators. With these special coupling paths, the order of the whole loop filter is increased. Meanwhile, this will also suppress idle tones in low order loop and provides dithering. Further performance improvement is achieved by adding time interleaving between those two modulators. Input feed-forward is used in each modulator, which enables the low OTA DC gain requirement of 50 dB only. With the supply voltage of 1.5 V, only 28 mW is consumed to achieve the conversion rate of 8.4 MS/s.

2.6 SAR ADC

2.6.1 Binary Search and the Basic Operation of SAR ADC

In computer science, a binary search [18] algorithm finds the position of a specified value within a sorted array. At each stage, the algorithm compares the input key value with the key value of the middle element of the array. If the keys match, then a matching element has been found so its index or position is returned. Otherwise, if the sought key is less than the middle element's key, then the algorithm repeats its action on the sub-array to the left of the middle element or, if the input key is greater, on the sub-array to the right.

A binary search halves the number of items to check with each iteration, so locating an item takes logarithmic time. It requires far fewer comparisons than a linear search, but it imposes the requirement that the list be sorted.

Successive approximation (SAR) ADC is a type of A/D converter that converts a continuous analog waveform into a discrete digital representation via a binary search through all possible quantization levels before finally converging upon a digital output for each conversion.

Although there are many variations for implementing a SAR ADC, the basic architecture is quite simple, which is shown in Figure 2.14. The analog input voltage V_{IN} is held on a track/hold element. To implement the binary search algorithm, the *N*-bit register is first set to midscale (that is, 100...00, where the MSB is set to 1). This forces the DAC output V_{DAC} to be $V_{REF}/2$, where V_{REF} is the reference voltage provided to the ADC. A comparison is then performed to determine if V_{IN} is less than, or greater than, V_{DAC}. If V_{IN} is greater than V_{DAC}, the comparator output is a logic high, or 1, and the MSB of the *N*-bit register remains at 1. Conversely, if V_{IN} is less than

V_{DAC}, the comparator output is a logic low and the MSB of the register is cleared to logic 0. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete and the *N*-bit digital word is available in the register.

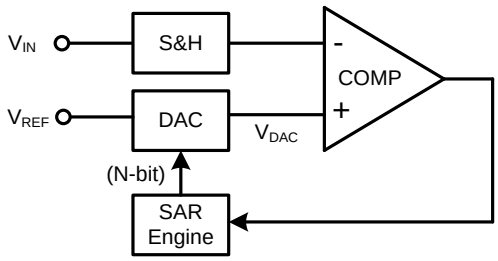

Figure 2.14: Basic building blocks of SAR ADC.

Figure 2.15 shows an example of a 4-bit conversion. The y-axis represents the DAC output voltage. In the example, the first comparison shows that $V_{IN} < V_{DAC}$. Thus, bit 3 is set to 0. The DAC is then set to 0100 and the second comparison is performed. As $V_{IN} > V_{DAC}$, bit 2 remains at 1. The DAC is then set to 0110, and the third comparison is performed. Bit 1 is set to 0, and the DAC is then set to 0101 for the final comparison. Finally, bit 0 remains at 1 because $V_{IN} > V_{DAC}$.

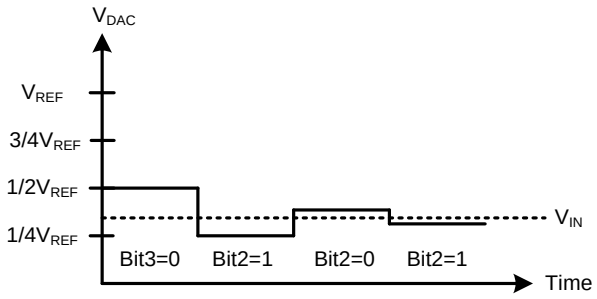

Figure 2.15: The operation of 4-bit SAR ADC.

2.6.2 Charge-redistribution SAR ADC

One of the most common implementations of the SAR ADC, the charge-redistribution SAR ADC [19], uses a charge scaling DAC. The charge scaling DAC simply consists

of an array of individually switched binary-weighted capacitors. The amount of charge upon each capacitor in the array is used to perform the aforementioned binary search in conjunction with a comparator internal to the ADC and the successive approximation register. One 4-bit binary capacitor array example is shown in Figure 2.16 ($C_4 = 2C_3$, $C_3 = 2C_2$, $C_2 = 2C_1$, $C_1 = C_0$). One important feature of this topology is to provide the sample-and-hold function inherently.

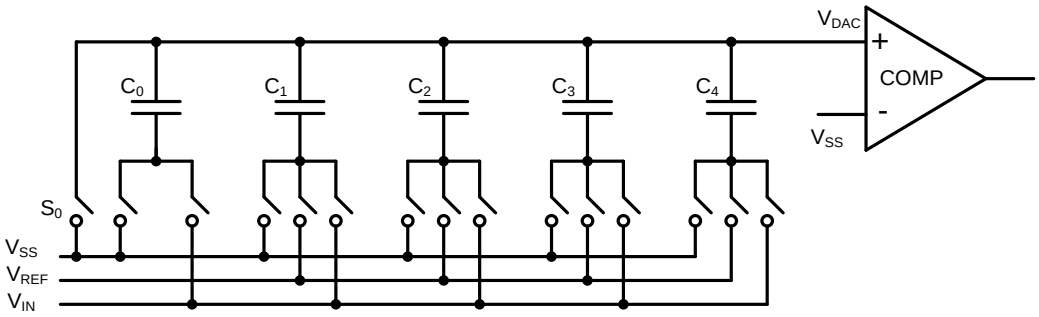

Figure 2.16: Charge-redistribution SAR ADC using binary capacitive array.

In [20], the split capacitor array is proposed, which is shown in Figure 2.17 ($C_4 = 2C_3$, $C_3 = C_0$, $C_2 = 2C_1$, $C_1 = C_0$, $C_b = 4/3C_0$).

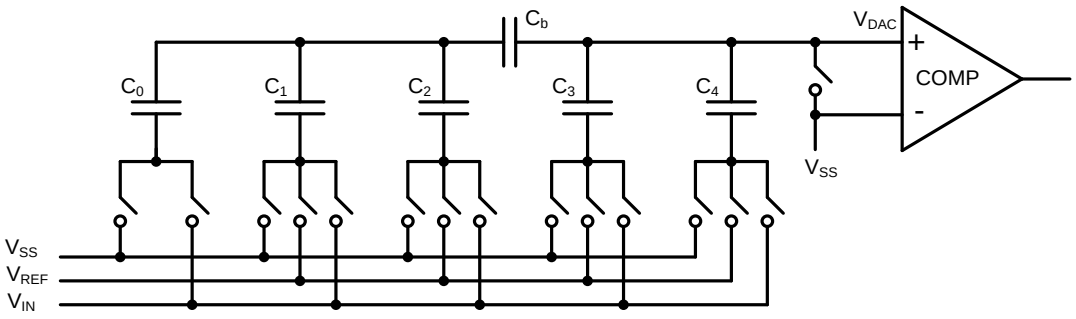

Figure 2.17: SAR ADC using split capacitive array.

With the split capacitor array, the number of unit capacitors is 8 for 4-bit DAC, compared with 16 units in binary one. This reduces the total capacitance and eases the layout design. One thing worthy to mention is that the size of unit capacitor in split array is larger than that in binary one. One example for 10 bit SAR ADC is listed in Table 2.3, in which the ratio of the unit capacitor is 8.

Table 2.3: Comparison for 10-bit capacitor array.

Array type	Unit capacitor	Num of Caps	Total size
Binary	C_u	1024	$1024C_u$
Split (5 bit + 5 bit)	$8C_u$	64	$512C_u$

2.6.3 Leakage Prevention during Successive Approximation

For the topology in Figure 2.16, the DAC output is forced to V_{SS} during input sampling. After the convergence of successive approximation, the DAC output goes back to V_{SS}. During SAR conversion, the DAC output may become negative, which forwardly biases the PN junction inside the sampling switch S_0. The resulted leakage will ruin the charge conservation and distort the conversion results.

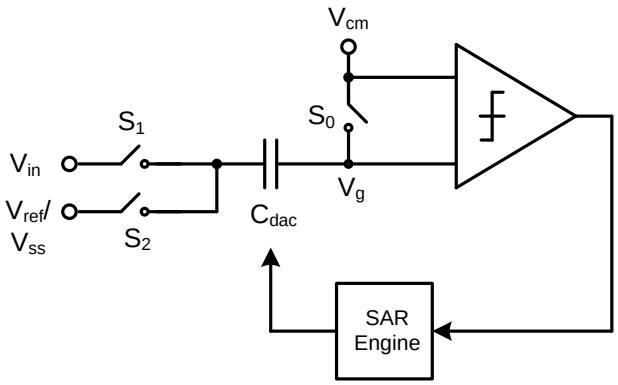

Figure 2.18: Leakage prevent during successive approximation.

This issue can be fixed by using a different V_{cm} voltage, instead of V_{ss}, as shown in Figure 2.18. During input sampling, V_g is forced to V_{cm}, which is its potential after SAR conversion. Due to the nature of binary searching algorithm, the SAR ADC is most prone to the leakage issue for the MSB period among the whole conversion. To decide the MSB, half of C_{dac} is connected to V_{ref}, another half is connected to V_{ss}. The input of comparator is set as

$$V_g = 0.5V_{ref} + V_{cm} - V_{in}. \quad (2.17)$$

So, the optimal Vcm is around half of V_{ref}, in order to prevent leakage with rail-to-rail input range.

2.7 Nonlinearity Analysis for SAR ADC

Differential non-linearity error (DNL) is the deviation of the step size of a real data converter from the ideal width of the bins Δ. Assuming that X_k is the transition point between successive codes $k-1$ and k, then the width of the bin k is $\Delta_r(k) = (X_{k+1}-X_k)$; the differential non-linearity is

$$DNL(k) = \frac{\Delta_r(k) - \Delta}{\Delta}. \quad (2.18)$$

The maximum differential nonlinearity is the maximum of |DNL(k)| for all k. Often the maximum differential nonlinearity is simply referred to as DNL.

Integral non-linearity (INL) is a measure of the deviation of the transfer function from the ideal interpolating line. Another definition of the integral non-linearity measures the deviation from the endpoint-fit line. The use of the endpoint-fit line corrects the gain and offset error. The second definition is chosen as standard since it is more informative for estimating harmonic distortion. The maximum of the INL is the maximum of |INL(k)| for all k. Often, it is referred to as just INL. One simple way to calculate the INL is

$$INL(k) = (1+G) * \sum_{i=1}^{k} DNL(i), \quad (2.19)$$

where, G is the gain error. It shows that the INL at bin k is the running sum of the DNL corrected by the gain error.

For the effect of INL and DNL on the FFT spectrum, a large DNL acts as a source of extra noise. Its running sum is added to the quantization and degrades the SNR. A large INL means large deviation of the transfer curve from the straight line thus causing harmonic distortion. Harmonic terms affect the SFDR and SNDR.

The resistor string DAC as shown in Figure 2.19 is one example of unit element one.

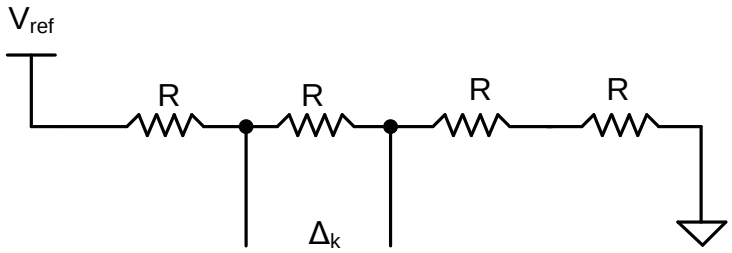

Figure 2.19: The unit element DAC.

The standard derivation of DNL can be calculated as

$$\sigma_{DNL} = \sigma_{dR/R}, \qquad (2.20)$$

where, $\sigma_{dR/R}$ is the standard derivation of resistor variation. That is to say, the DNL of unit element DAC is independent of resolution. The INL can be calculated as

$$\sigma_{INL} = \frac{1}{2}\sqrt{2^N - 1} * \sigma_{dR/R}, \qquad (2.21)$$

where, N is the number of DAC bits. The INL of unit element DAC is a function of resolution. The thermometer decoding is a usual way to achieve the unit element DAC.

For the binary weighted DAC, the worst DNL error occurs at middle scale. It can be calculated as

$$\sigma_{DNL} = 2^{N/2} * \sigma_e, \qquad (2.22)$$

where, N is the number of DAC bits. The INL can be calculated as

$$\sigma_{INL} = \frac{1}{2} * 2^{N/2} * \sigma_e = \frac{1}{2}\sigma_{DNL}. \qquad (2.23)$$

As above, the unit element DAC achieves same INL as the binary weighted one while much smaller DNL error. However, the implementation of unit element one is more complex. Normally, the DAC inside the SAR ADC is a combination of these two.

2.8 Test Method for DC Performance of SAR ADC

In the ramp approach, a histogram of code occurrences is generated in response to an input signal level which ramps linearly between the extremes of the full-scale range of the ADC. After a sufficiently large number of samples, the histogram of the output provides an accurate measure of the differential nonlinearity (DNL) of the ADC. Integral nonlinearity can be directly computed by numerically integrating the differential nonlinearity data. The input ramp shall be generated synchronously with the sampling clock, by a high-resolution DAC or arbitrary waveform generator with suitable linearity. Absolute signal level measurements can be made at the terminal codes to compute offset and gain errors.

The precision of the measured values of the code transition levels depends on the total number of histogram samples measured. Increasing the number of samples decreases the uncertainty while ramping the input. A larger total number of samples reduce the uncertainty. Nonlinearity of the ramp input signal would produce errors in the code transition levels. Noise on the ramp signal or the ADC under test will cause uncertainty in the measured code transition levels. Specifically, the uncertainty in LSBs due to noise in the estimate of a transition level is approximated by

$$\varepsilon = \frac{\sigma_N}{\sqrt{H}}, \qquad (2.24)$$

were, σ_N is standard deviation of the noise, in units of ideal code bin widths (LSBs), H is the average number of histogram samples received in each of the code bins.

The ramp method is generally used when static characteristics of the device under test are being measured. The sine-wave histogram is generally used for dynamic testing. The ramp method is more efficient in measuring the device characteristics. Histogram methods can produce erroneous results if the device being tested has output codes that are swapped with other codes or exhibits other types of non-monotonic behavior. Such converters can produce seemingly good results, yet have large errors in the actual code transitions. To avoid these issues, converters should also be tested for SNDR performance to confirm that non-monotonic behavior is not significant.

Another widely used test method for determining transition levels is based on a feedback loop. In this method an input is applied to the ADC, the converter is triggered, and the results of the conversion are compared to a desired value. If the ADC output is below the desired value, the input is raised by a fixed amount. If the ADC output is equal to or above the desired value, the input is lowered by a fixed amount. This process is repeated until the ADC input has settled to a stable, average value. In this method, a feedback loop is used to adjust the ADC input, until there is equal chance to get the results above (and include) and below a certain digital code.

In an ideal noiseless ADC, repeated tests with smaller values of input step size can determine the transition level as precisely as desired. In a real-world ADC, one with internal noise, the situation becomes more complex because the noise affects the properties of the asymptotic state of the test. One way is to look at the statistical distribution of the digital outputs. The transition voltage can be identified with digital results 50% above (include) and below a certain code.

Also, a pure sine wave of amplitude sufficient to slightly overdrive the ADC is input to the ADC under test. The frequency of the sine wave and the ADC sampling frequency shall be specified. Multiple records of ADC output data are taken and a

histogram constructed. One exampled histogram with sine wave input is shown in Figure 2.20. From that, the DNL and INL can be calculated.

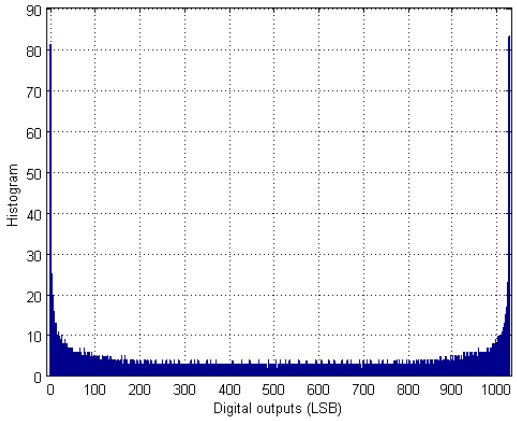

Figure 2.20: The histogram method with sine wave inputs.

2.9 SAR ADC in Literature

With demand on low power consumption, the SAR ADC is attracting more and more attentions due to its high power efficiency. To get an overview of the research status in low power SAR ADC, the literature review is performed within the papers from JSSC and ISSCC published from 2007 to 2011. It is summarized in Table 2.4.

Table 2.4: The literature searching for SAR ADC.

Index	Style	Res. (Bit)	VDD (V)	Speed (MS/s)	INL/ DNL (LSB)	Tech. (um)	FOM fJ/conv.	Source & Year
[21]	Diff.	5~10	0.4~1	~2	0.57/0.58	0.065	22.4	ISSCC, 11
[22]	Diff.	8	1	10	0.90/0.90	0.090	12	JSSC, 11
[23]	Diff.	10	1.2	40	1.55/0.78	0.13	50	JSSC, 11
[24]	Diff.	10	1.0	1	2.24/0.49	0.065	4.4	JSSC, 10
[25]	Diff.	10	1.2	100	0.86/0.79	0.09	55	JSSC, 10
[26]	Diff.	10	1.2	50	1.36/0.91	0.13	29	JSSC, 10
[27]	Diff.	10	1.0	50	0.72/0.82	0.065	30	ISSCC, 10
[28]	Single	12	1.0	0.1	2.50/2.00	0.18	56	ISSCC, 08
[29]	Single	8	0.9	0.2	0.53/0.90	0.18	65	JSSC, 07
[30]	Diff.	6	0.5	1.5	0.60/0.70	0.09	140	JSSC, 07
[31]	Diff	12	1.0	0.2	0.19/0.16	0.18	165	JSSC, 07

In [21], a resolution reconfigurable 5-to-10b 0.4-to-1V power scalable SAR ADC is presented. Instead of truncating the unused bits for different resolution, a reconfigurable DAC improves the power scaling with resolution. It is achieved by adding some boosted switches inside the capacitor array, in order to avoid attenuation at the DAC output due to those unused MSB capacitors. The DAC uses reconfigurable 1-to-6b main split-capacitor array to lower DAC switching energy and a 4b sub-DAC to reduce area. The common mode reference is eliminated by using differential capacitor array. The comparator does not include any pre-amplifier; some

compensating circuit is employed to reduce the offset error. Power gating is used to reduce the leakage during sleep mode.

In [22], a 26 μW, 8 bit, 10 MS/s, asynchronous SAR ADC is presented. Top plate sampling is adopted for the differential capacitor network (or array). A customized unit capacitor of 0.5 fF is modeled using an in-house extraction tool and used to build the DAC. Capacitor mismatch is also estimated by Monte Carlo simulation. Dynamic comparator is used and the offset error is affordable. In order to reduce the power from digital portion, asynchronous dynamic logic is applied to the SAR engine design. This paper is solid in fundamental, concept and calculation. Please notes, the same work is presented in ISSCC 2010.

In [23], a 550 μW, 10-bit, 40 MS/s SAR ADC is proposed. The key idea is to use a multistep addition-only digital error correction (ADEC) technique to increase the conversion speed, with some redundant decision cycles. The conversion speed is increased by 37% in a 10-b ADC with negligible hardware overhead. Meanwhile, this paper provides a good summary of recently published SAR ADCs, with four categories.

In [24], a 1.0 V, 1 MS/s, 10-bit SAR ADC is presented. The most impressive idea is the step-wise charging for the charge redistribution DAC. Step-wise charging with one or multiple intermediate steps in between ground and the reference voltage can be used to reduce the energy dissipation. The intermediate voltages are stored in the big auxiliary capacitors, which consumes large silicon area. A dynamic two-stage comparator and a delay-line-based controller are also adopted for low power consumption. With the power consumption of 1.9 μW, this ADC achieves an energy efficiency of 4.4 fJ/conversion.

In [25], a 1.2 V 10-bit 100 MS/s SAR ADC is presented. The reference generator is eliminated by directly using the supply voltage as the reference voltage. A passive gain by 2 of the input is implemented to compensate the effective SNR degradation due to higher reference. The switching energy saving technique avoids the mismatch error at the conventional most significant bit (MSB) transition and enables a reduction by 2 of the overall capacitance used in the SAR. The charge recovery, implemented during each bit cycling, cuts by 1/3 the switching energy. One drawback is it requires a dedicated Vcm voltage to implement charge recovery. With the power consumption of 3 mW and ENOB of 9.1bit, this ADC achieves the FoM of 55 fJ/conversion.

In [26], a 1.2 V 10-bit 50 MS/s SAR ADC is presented. The proposed monotonic switching method reduces power consumption by 81% without splitting or adding capacitors and switches. The total capacitance in the DAC capacitor network is reduced by 50%. In addition, the switching method improves the settling speed of the DAC capacitor network. This paper also presents an improved comparator design to avoid the linearity degradation, in which a current source is added into the dynamic latched comparator. With the power consumption of 0.82mW and ENOB of 9.1, this ADC achieves the FoM of 29 fJ/conversion.

In [27], a 10b 50MS/s 820μW SAR ADC is presented. A 50MHz external clock with 25% duty ratio is required. The analog signal is sampled during clock high period and converted during clock low period. Body biasing technique is applied to the input differential pair of the dynamic latch comparator. This method does not reduce the comparator's speed like other trimming methods. The capacitor array is designed to reduce the capacitive load to its input. Also, the nonlinearity due to capacitor mismatch is compensated by digital calibration. With the supply voltage of 1.0 V and power consumption of 820 μW, this ADC achieves the FoM of 30 fJ/Conversion.

In [28], a 9.4-ENOB 1.0 V 3.8 μW 100 kS/s SAR ADC is presented. The most attractive idea is to use the time-domain comparator. Before comparison, two capacitors are pre-charged to VDD. The input voltage and the DAC output are mapped into two currents, which are used to discharge the two capacitors respectively. One DFF is utilized to reveal the pulse that ends first and provides the comparator output. The binary-weighted split-capacitive arrays are used in this ADC. The value of the scaling capacitance between the two arrays is one instead of being fractional; this cause minor gain error. This ADC achieves the FoM of 56 fJ/conversion.

In [29], a 0.9-V 200-kS/s rail-to-rail 8-bit SAR ADC is presented. It is based on the most conventional topology of SAR ADC, in which the output from the track-and-hold circuit and the output from DAC are connected to two inputs of the comparator. The parasitic capacitor at the DAC output will impact the ADC results. Also, the comparator needs to support rail-to-rail input range. A bootstrapped switch is used for the track-and-hold circuit; the comparator is composed of a NMOS differential input pair and a PMOS differential input pair. With the power consumption of 2.47 μW and the ENOB of 7.58, this ADC achieves the FoM of 65 fJ/conversion.

In [30], a 0.5 V, 1.5 MS/s, 6-bit SAR ADC is presented. This design uses top-plate sampling, which causes some nonlinearity of the parasitic capacitance on the top plate. Due to the small size of the active devices used, the parasitic capacitance on the top plate of the array is dominated by routing and is hence quite linear for 6-bit resolution. A binary-weighted 1.5 b/element design is used, which reduces the total capacitance from 63 unit capacitors to 31 unit capacitors. For the comparator design, a cascoded device is introduced to the input pair to reduce the kick-back noise, while a small capacitor bank is adopted to reduce the comparator offset error. With power

consumption of 7 μW and the ENOB of 5.15, this ADC achieves the FoM of 140 fJ/conversion.

In [31], a 1.0V, 100 kS/s, 12-bit SAR ADC is presented. This resolution-rate scalable ADC for micro-sensor networks supports both 12-bit and 8-bit modes. Meanwhile, this ADC can sample both differential and single-ended inputs. The CMRR is enhanced by common-mode independent sampling and passive auto-zero reference generation. For the comparator, the path for 12-bit mode has three cascaded preamplifiers, while the path for 8-bit mode has only one pre-amplifier. The most impressive point in this work is the offset compensating latch. The trimming is completed in analog style, instead of conventional digital way. With power consumption of 12 μW and the ENOB of 10.55, this ADC achieves the FoM of 165 fJ/conversion.

CHAPTER 3 A 1-V, 82-DB, 2.5-MS/S, SINGLE BIT DELTA-SIGMA MODULATOR

3.1 Introduction

With the evolution of wireless and wire-line communication systems, analog-to-digital converters with 13 ~ 14-bit resolutions and over 1-MHz signal bandwidth are in great demand. Meanwhile, the CMOS feature size is scaled down and the supply voltage is reduced continuously. All these factors make ADC design challenging.

In deep sub-micron CMOS technologies, the supply voltage is decreased. The reduced supply voltage makes it difficult to design high-performance Delta-Sigma ADCs. The main difficulty is the small signal swing constrained by the reduced supply voltage and the degradation of the transistor characteristics. With sub-micron process, it is more difficult to achieve high DC gain from OTA.

In [8], a feedforward Delta-Sigma modulator with the conversion rate of 25-Ms/s is presented, however, the supply voltage is limited at 1.8V and it consumes 200-mW in total. To overcome the finite gain effect, gain boosting technique is utilized in the first OTA, which consumes about 26% of the total power. In [11], a cascoded Delta-Sigma modulator with multi-bit quantizer is described. Although implemented in 0.13-μm CMOS process, the power consumption from digital portion is fairly high. Complex DWA and error cancellation logic are required to achieve high accuracy. Meanwhile, to leave enough output swing for the integrator output, the OTA is implemented with folded cascoded topology, which is less power efficient as the telescopic one. In [16], to improve the power efficiency, a split-path pseudo-differential amplifier is

proposed. However, the harmonic distortion is very obvious in the output spectrum, which results in large difference between SNR and SNDR from the measurement results.

Circuit-level problems may be easily solved on system level. As a full system, the signal swing inside the Delta-Sigma ADC can be minimized by system level optimization. The input feedforward Delta-Sigma topology [32] is a perfect candidate for Delta-Sigma ADC designs in deep sub-micron CMOS technologies. Firstly, the signal transfer function of this topology is unity, which is irrelevant to the loop-coefficients. OTA with low DC gain can be adopted without degrading the conversion accuracy. The quantization noise transfer function remains the same as the one of the traditional topology, a single loop topology without feedforward. Secondly, the internal signal swing can be well suppressed by optimizing the loop coefficients. It is possible to use the OTA topology with high power efficiency, such as telescopic one. Besides, there is only one feed-back signal to the first integrator, which simplifies the circuit implementation compared to the traditional topology.

3.2 Architecture Design

Traditionally, Delta-Sigma modulator is used for low frequency conversion. For the ADSL system, the required conversion rate is 2.5 Ms/s. To get higher conversion rate, one can either increase the sampling frequency or reduce the oversampling ratio (OSR). It is possible to achieve low OSR with multi-stage loop filter or multi-bit quantizer [7]. Although the multi-stage topology can ease the stability issue for high order Delta-Sigma modulator, high OTA DC gain is required to get a good cancellation for the quantization noise from 1^{st} stage [33]. It becomes more and more difficult to design a high gain OTA with deep sub-micron processes and low supply voltage.

Multi-bit Delta-Sigma modulators also have some drawbacks with low supply voltage. First, the reference level is limited to the supply voltage. To get large dynamic range, it is valuable to set the reference equal to supply voltage. This will make design of multi-bit ADC and its pre-amplifier fairly difficult [34]. For the input feed-forward Delta-Sigma modulator, the situation is even worse, because the nonlinearity of the active summing circuit and ADC's pre-amplifier is not attenuated by loop NTF (noise transfer function). However, for the single-bit design, passive summing circuit can be used with much less design complexity and implicit linearity. Secondly, the dynamic range of multi-bit Delta-Sigma modulator is limited by the accuracy of feedback DAC. Normally, dynamic element matching (DEM) is used to improve the linearity. However, it increases the delay in the feedback path. For the input feed-forward Delta-Sigma modulator, normally the time slot assigned to DEM is very short. In [35], a split reference feedback method is proposed to relax the timing requirement. However, the mismatch between the two paths will cause some nonlinearity. Area and power is another consideration for DEM. In [8], the power consumption for DEM is 6mW, with the clock speed of 200 MHz. To operate the calculation-intensive DEM at such a high frequency, the area is not small. With the estimated power dissipation capacitance of 20 pF ($1/2fCV^2$), the number of gates is about 8, 000 for 0.18-μm process.

With deep sub-micron processes and low supply voltage, the Delta-Sigma modulator with single-bit quantizer and single-stage loop filter has some advantages. First, the single-bit DAC is implicitly linear. No DEM is required. Secondly, it is much easier to design a single-bit quantizer. Its offset error is not as critical as that in a multi-bit design. Dynamic latch without pre-amplifier can be used safely. So the design complexity is reduced significantly. Meanwhile, the input feedforward Delta-Sigma

topology does not require high DC gain and large output swing from OTA, which is the main building block for Delta-Sigma modulator.

To achieve the dynamic range of 80 dB, one single-loop, single bit, 4^{th}-order loop filter is implemented, with over-sampling ratio (OSR) of 64. The topology is shown in Figure 3.1, in which I(z) is the z-domain transfer function of non-inverting switched capacitor integrators, i.e.,

$$I(z) = \frac{z^{-1}}{1 - z^{-1}}. \qquad (3.1)$$

For 0.13-μm process, it is feasible to set the sampling frequency as 160-MHz. With such a high sampling frequency, critical demand on clock jitter specification is the main drawback for the continuous time Delta-Sigma modulator. In [8], to achieve the targeted SNR of 90 dB, the calculated maximum jitter is 0.09 ps for continuous time case, compared with 0.9 ps for discrete time one. Because of the relaxed requirement on clock jitter, discrete-time design is adopted for this implementation.

For this loop filter, the input signal is also fed to the summing circuit before quantizer with gain of 1. Different gain is assigned to the outputs of each integrator. The output of the quantizer is only fed back to the first integrator. This simplifies the circuit design compared with conventional feedback topology, in which the quantizer output is fed back to the inputs of every integrator.

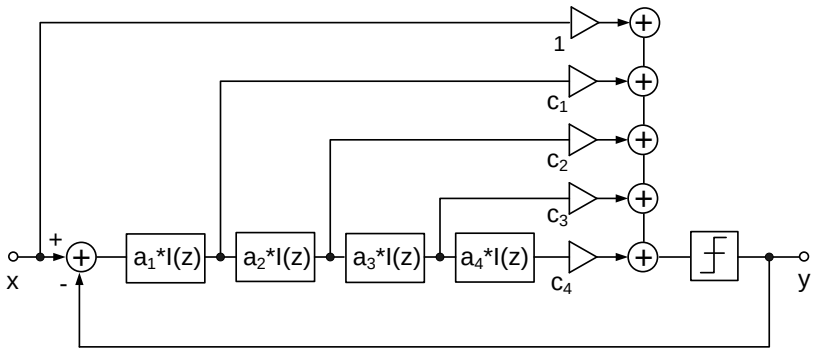

Figure 3.1: Block diagram of the proposed modulator.

Behavioral simulation with MATLAB is used to optimize the filter coefficients [36] [37]. In this implementation, [a_1 a_2 a_3 a_4] = [0.2 0.4 0.1 0.1] and [c_1 c_2 c_3 c_4] = [1 1 1 2]. The outputs of different integrator stages and output spectrum with Fin of 50 kHz are plotted in Figure 3.2 and Figure 3.3 (input frequency of 50 kHz). In the MATLAB behavioral simulation, the finite DC gain from OTA is modeled and the kT/C thermal noise is added.

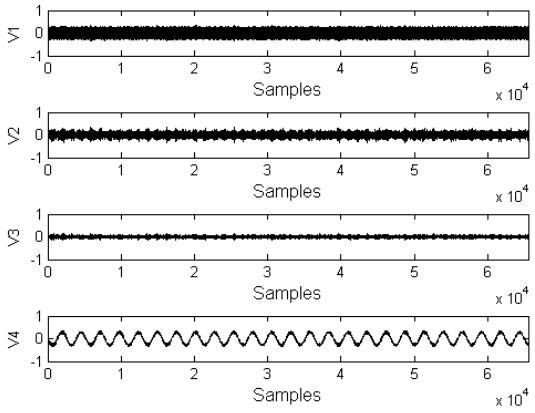

Figure 3.2: Integrator outputs from the proposed modulator.

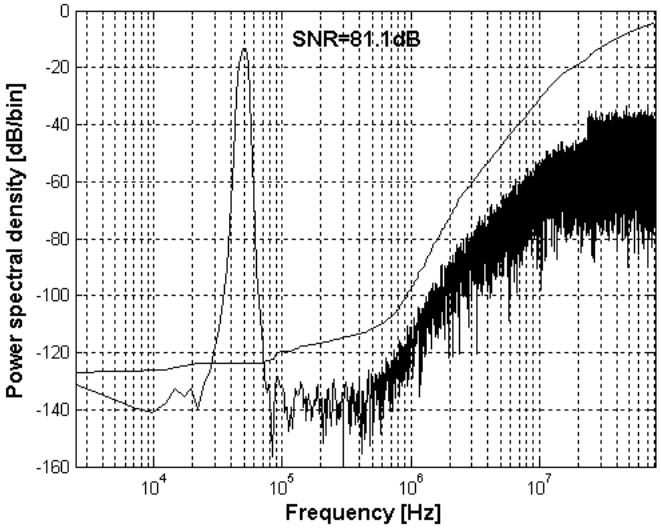

Figure 3.3: Output spectrum from the proposed modulator.

As a comparison, the integrator outputs from the traditional 4th-order feedback Delta-Sigma loop are shown in Figure 3.4. Much larger output swing is required for the

building OTAs. The advantage of low output swing with input feed-forward topology is obvious.

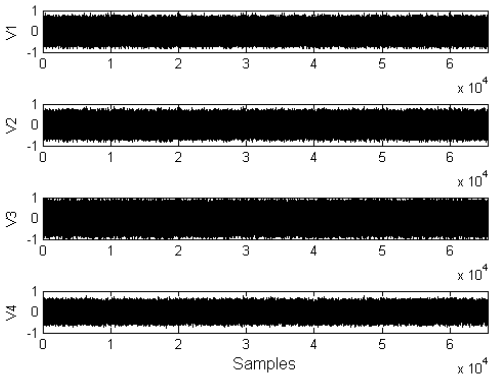

Figure 3.4: Integrator outputs from the traditional feedback modulator.

From MATLAB behavioral simulation, the effective gain from the quantizer is extracted using

$$k = \frac{E < v, y >}{E < y, y >}, \qquad (3.2)$$

where, y and v is the quantizer input and output. With input amplitude of 0.7, the quantizer gain k is calculated as 5.6477. The root-locus plot is shown in Figure 3.5. With large enough k or input amplitude smaller than 0.7, the loop filter is stable.

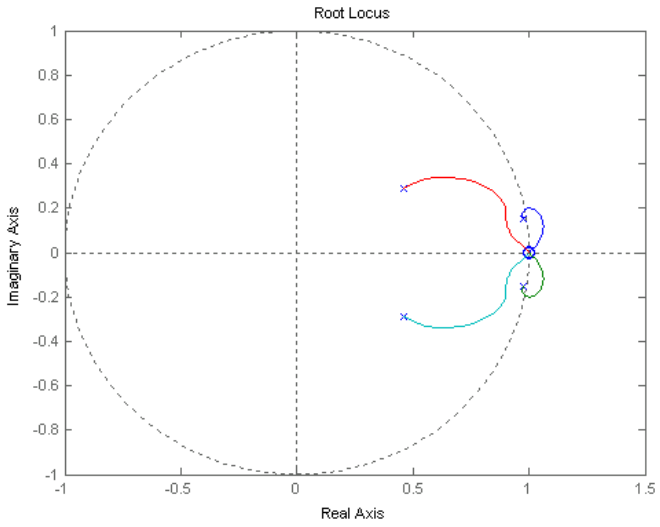

Figure 3.5: The root-locus plot for the loop filter.

For the proposed 4th-order modulator, it is possible to add zero-optimization to improve the quantization noise attenuation. After adding a feedback path from the 4th integrator to the 3rd one, the achieved output spectrum (without kT/C noise) is shown in Figure 3.6. The applied feedback coefficient is 0.02, which is obtained from multiple behavioral simulations. Please note the zero optimization is not included in silicon due to tape-out schedule.

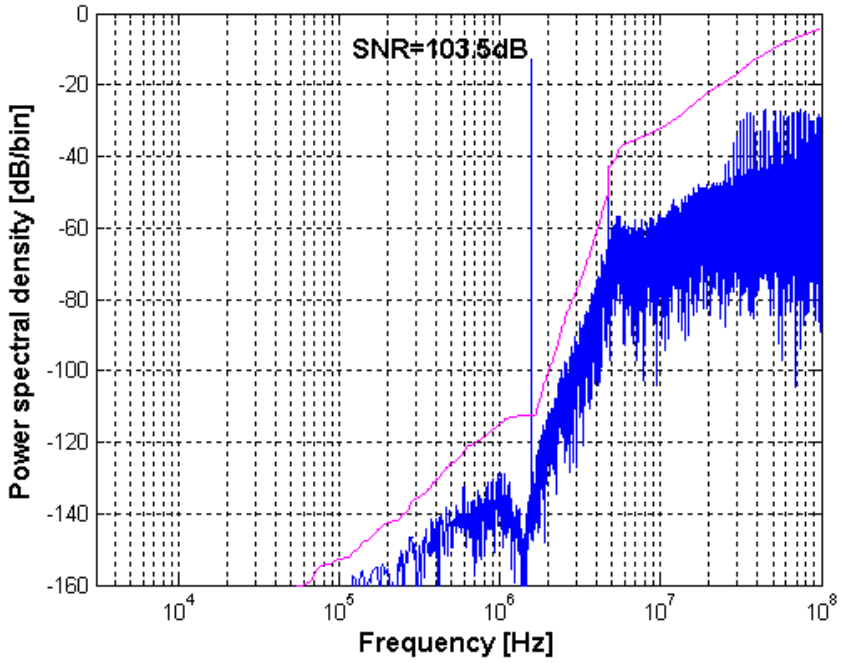

Figure 3.6: The output spectrum after zero optimization.

3.3 Switch Level Design

The switch level design is shown in Figure 3.8. Four parasitic-insensitive switched-capacitor integrators are the main components in the design. The capacitors size for different integrators is listed in Table 3.1. The capacitor size and OTA current are scaled down for the 2nd, 3rd and 4th integrator to save power. The scaling is based on

the transfer function from internal node to the modulator output, which is shown in Figure 3.7.

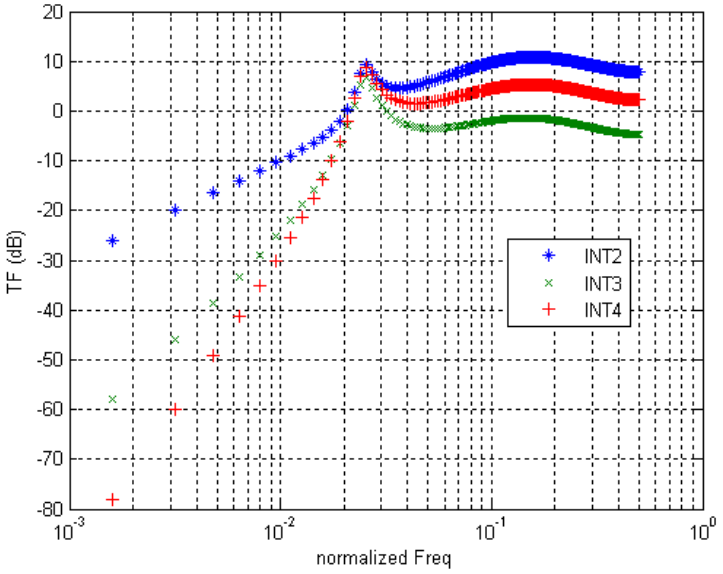

Figure 3.7: The transfer function from internal nodes to modulator output.

Table 3.1: Capacitor size for different integrators

Index of integrators	C_s (pF)	C_i (pF)	C_f (pF)
0			0.5
1	4	20	0.5
2	2	5	0.5
3	1	10	0.5
4	1	10	1

The feed-forward paths are implemented using passive switched capacitor summing circuit, which has an attenuation term of ΣC_{fi}, as shown in

$$Y(z) = \frac{\sum_{i=1}^{n} X_i(z) \bullet C_{fi}}{\sum_{i=1}^{n} C_{fi}}, \qquad (3.3)$$

where, X_i is the output of i-th integrator, C_{fi} is the *i*-th summing capacitor in Figure 3.8. However, for single-bit Delta-Sigma modulator, there is no need to compensate the attenuation as the quantizer needs the polarity information only and the amplitude information is not utilized.

For the switched-capacitor integrators, the input and output common mode voltage of the OTA are set to different value, which relaxes the requirement of input common mode range for low voltage design.

The strobe clock for the quantizer is right before the falling edge of c_1. This will leave enough time for the passive summing circuit to settle, while minimizing linearity degradation due to clock slack. The output of the quantizer is only fed back to the first integrator. For high speed operation, there is only one switch between the reference voltage and the sampling capacitors of 1st integrator.

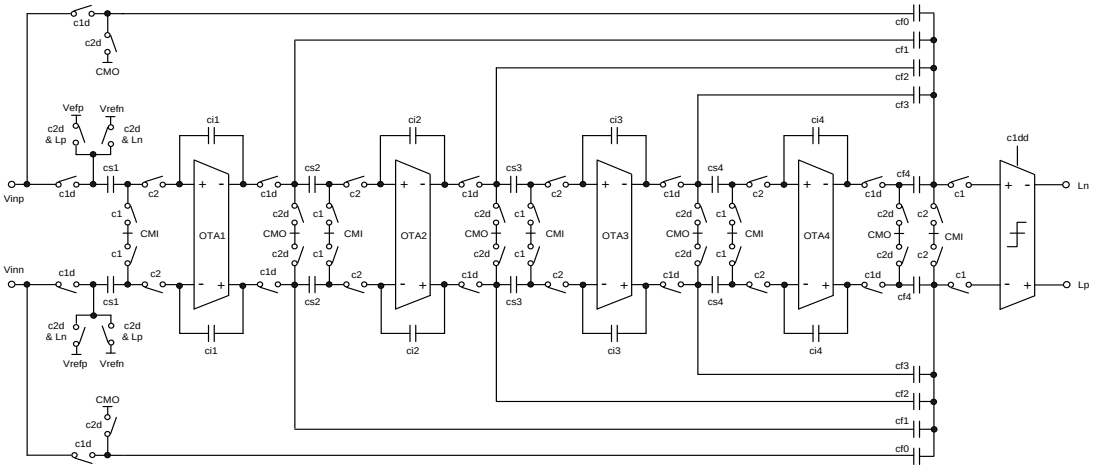

Figure 3.8: Schematic of the proposed modulator.

3.4 Circuit Implementation

3.4.1 OTA Design

OTA is the most challenging building block in high speed Delta-Sigma modulator. Its performance will limit the settling accuracy of switched-capacitor integrator, which will decide the dynamic range of the whole Delta-Sigma modulator. With the

sampling frequency of 160 MHz, the integrator is required to settle to adequate accuracy within 3 ns. To get the first order settling, telescopic configuration is used. The main drawback of this topology is the limited output swing compared with folded cascode one. However, it is forgivable for the input feed-forward topology. Meanwhile, folded cascode configuration will consume almost two times current to get similar performance. The schematic of OTA with biasing circuit is shown in Figure 3.9. NMOS input device is used here for high speed operation. The cascoded transistors are biased for wide output swing to reduce the gain non-linearity [38]. The simulated OTA DC gain is only 43 dB. For ease-of-integration and low power consumption, switched-capacitor CMFB [39] is adopted here.

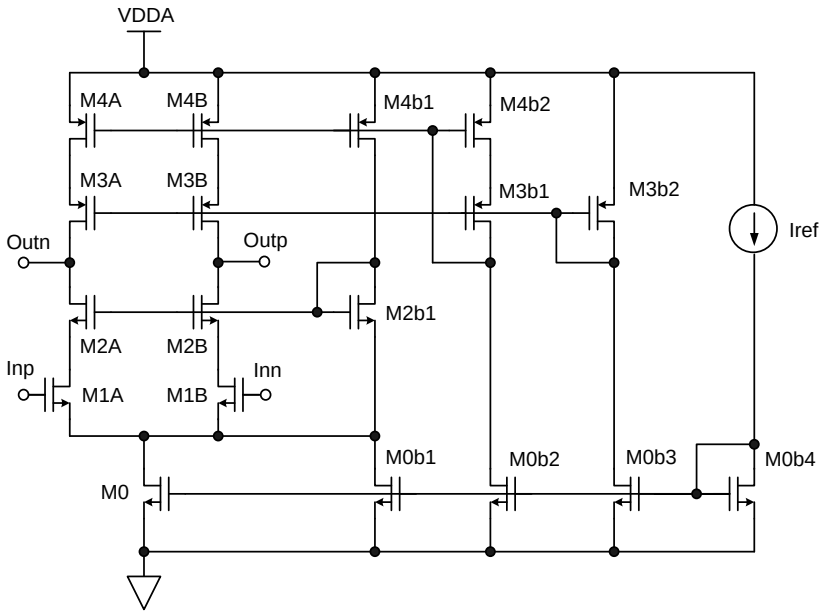

Figure 3.9: Schematic of the OTA.

3.4.2 Quantizer

For single-bit Delta-Sigma modulator, the offset from quantizer are not so critical. As shown in Figure 3.10, the comparator is composed of one dynamic latch with another SR latch. Because there is no static current flowing, low power consumption can be achieved for this comparator.

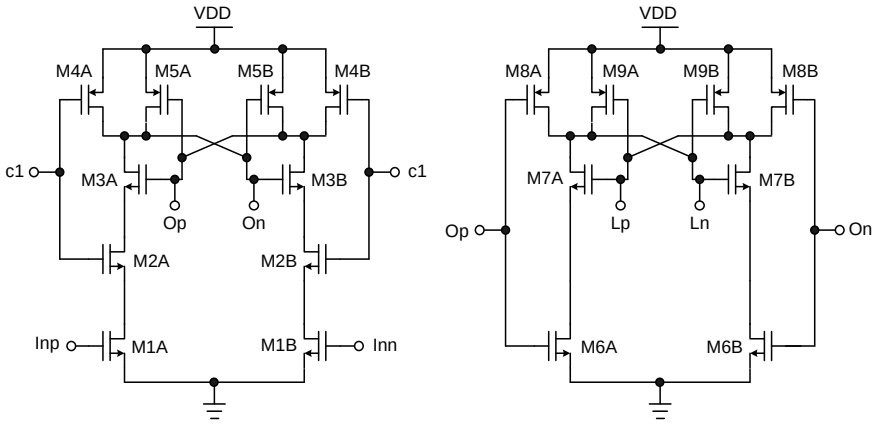

Figure 3.10: Schematic of the single bit quantizer.

3.4.3 Switches

The on resistance of the switches will impact the settling of the switched-capacitor integrators. To get better linearity at low voltage, bootstrapped technique [40] is used in this design, as shown in Figure 3.11. The transistors are sized carefully to reduce the clock feed-through and charge injection error.

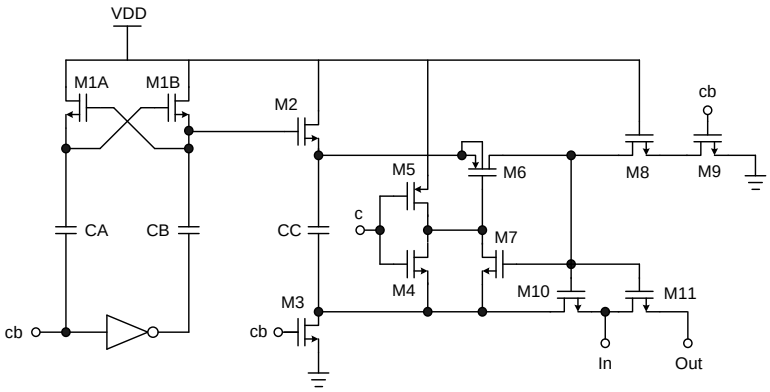

Figure 3.11: Schematic of the bootstrapped switch.

3.4.4 Differential Output Buffer

To reduce substrate coupling and noise on power bus, a differential output buffer, shown in Figure 3.12, with constant supply current is used. Compared to that used in [41], a small overlap is purposely added between those two control signals on the gates of output transistors, to reduce the amplitude of ripples in the supply current. Meanwhile, one on-chip serial-to-parallel converter is implemented.

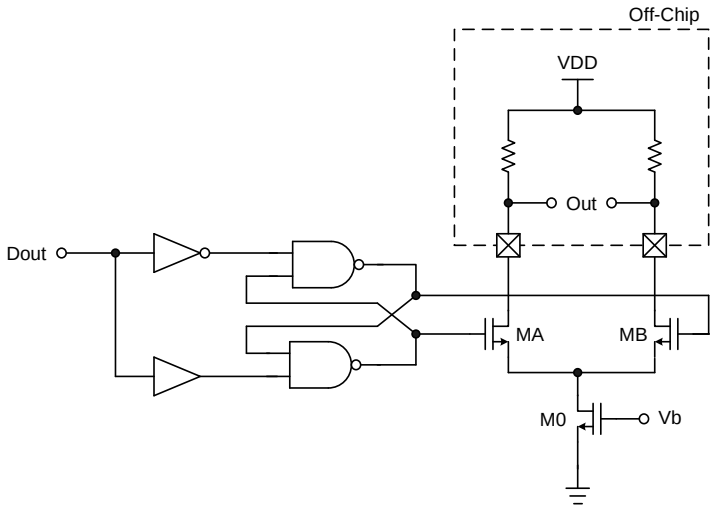

Figure 3.12: Schematic of differential output buffer.

3.4.5 Biasing Of Guard Rings

Biasing of guard rings is an important topic for high speed mixed signal design [42]. To reduce the substrate coupling from digital portion to analog portion, the biasing scheme in Figure 3.13 [43] is adopted here. For the transistors in digital portion, a guard ring biased with a dedicated ground pin provides a low resistance return path for the noise injected from the digital blocks, especially the high speed output buffer. This ring can not be biased with either digital ground or analog ground. Biasing with the digital ground would inject more noise into substrate, while using the analog ground would ruin itself.

For the transistors in analog portion, substrate noise disturbs the analog transistors mainly through the body effect. To reduce this coupling, bulk-source voltage variations of analog transistors should be minimized. The bulk is tied locally to the analog ground rather than to another dedicated ground.

Between the analog and digital portions, one guard band is inserted to reduce the interference further. This guard band is biased with another dedicated ground pin.

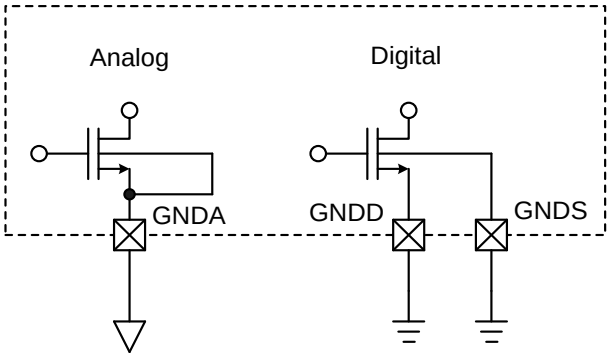

Figure 3.13: Guard ring biasing scheme.

3.5 Experimental Results for First Revision

The layout floorplan is shown in Figure 3.14. The four integrators are placed horizontally from left to right. The fully differential OTAs sit at the middle of the positive and negative portion of capacitors. The advantages are good symmetry and easy layout. However, the OTAs are surrounded by the noisy switches. Guard rings are used to minimize this effect. Another drawback of this floorplan is large mismatch between “CAP P” and “CAP N”. This does not change the filter coefficients between positive and negative portions. However, the absolute capacitor size does not match well between positive and negative portion, which degrades the supply rejection.

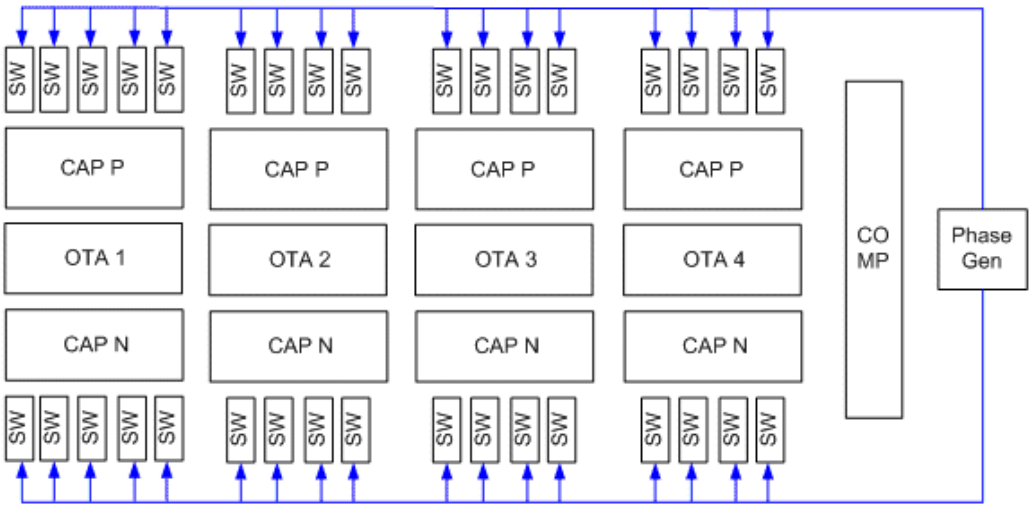

Figure 3.14: Layout floorplan for the first revision.

The layout view and pin out are shown in Figure 3.15 and Figure 3.16.

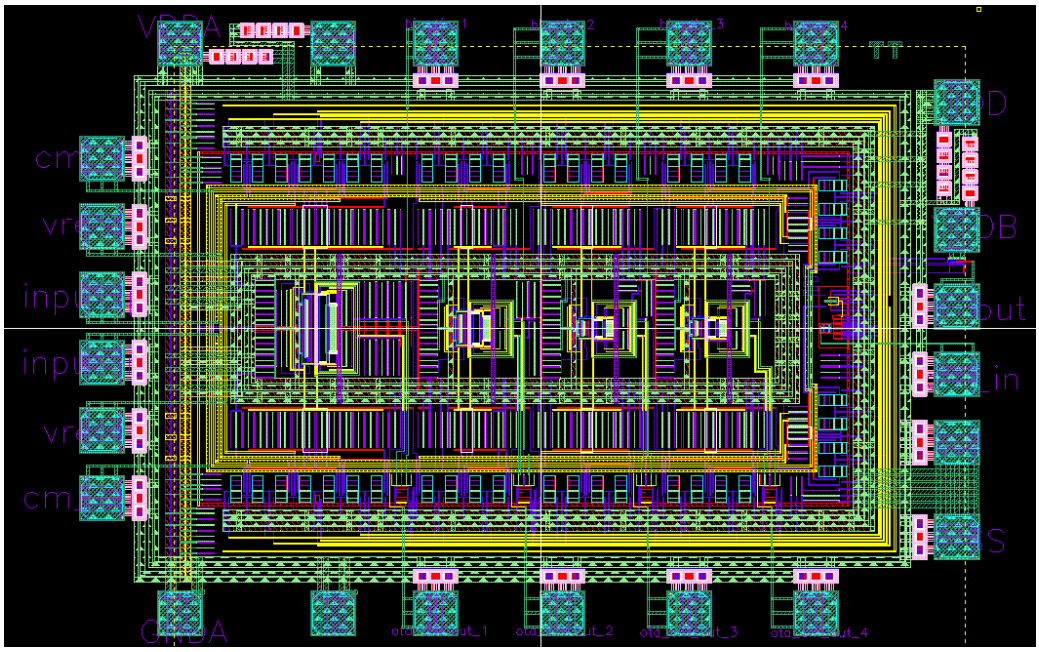

Figure 3.15: The layout view for first revision.

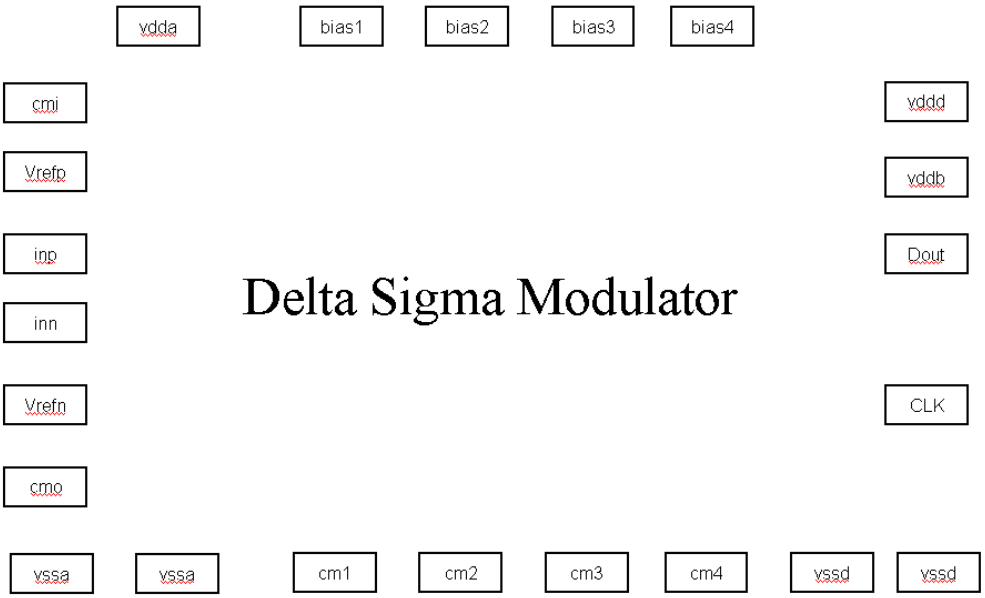

Figure 3.16: The pin assignment for first revision.

The chip is fabricated in TSMC 0.13 um digital process. The die photo is shown in Figure 3.17. Those four integrators are layout from left to right. The clock generator and the quantizer are at right hand side. The die size is 2mm X 1.5mm including the pad ring.

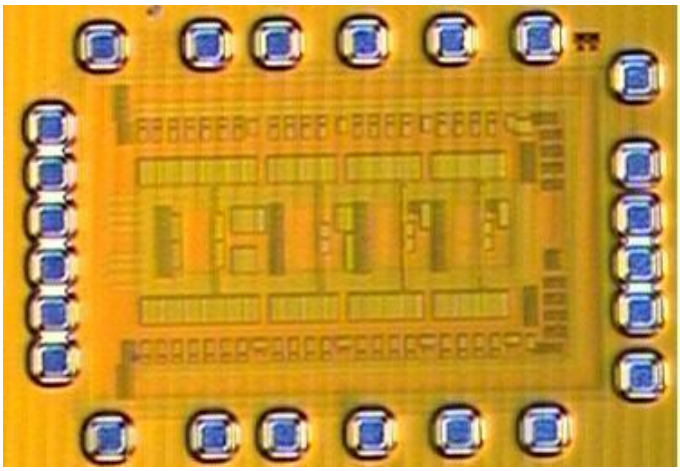

Figure 3.17: The Die Photo for first revision.

The modulator chip was bonded onto PCB directly, which is shown in Figure 3.18. It increases the difficulty in the debugging and limits the optimization in the PCB design.

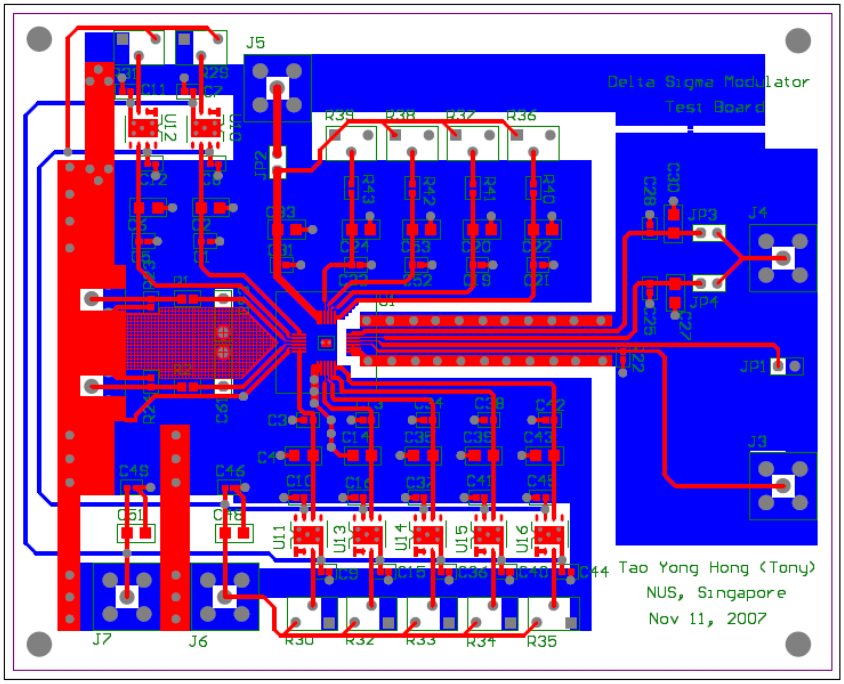

Figure 3.18: The PCB design for first revision.

The test setup is shown in Figure 3.19. An ultra-low-distortion signal source (DS360) is used to supply the fully differential input signal. Agilent 8133A provides the clock source.

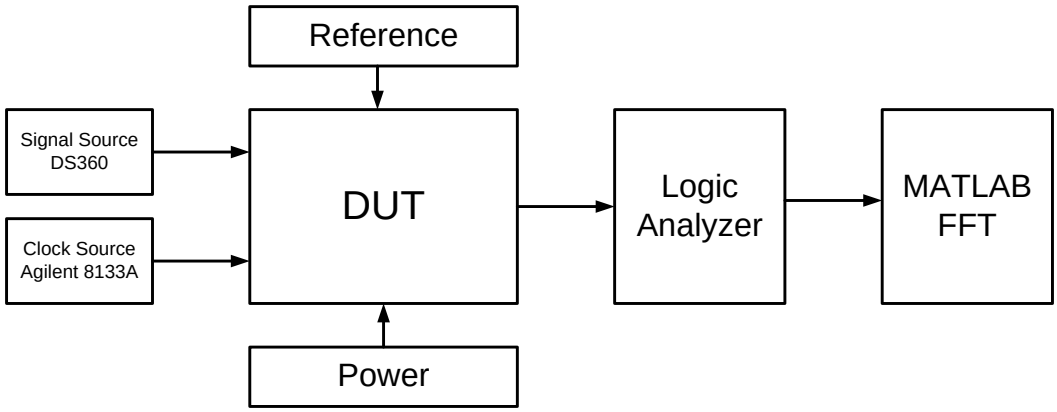

Figure 3.19: The test setup for first revision.

Clocked at 50 MHz, the modulator consumes 35 mW (30 mW in analog and 5 mW in digital). The design target is to run the modulator at 200 MHz. However, the conversion speed is limited due to implementation issue, such as substrate coupling and crosstalk in PCB (long bonding wire to PCB directly). A measured peak SNDR (harmonic included) of 81.6 dB is plot in Figure 3.20.

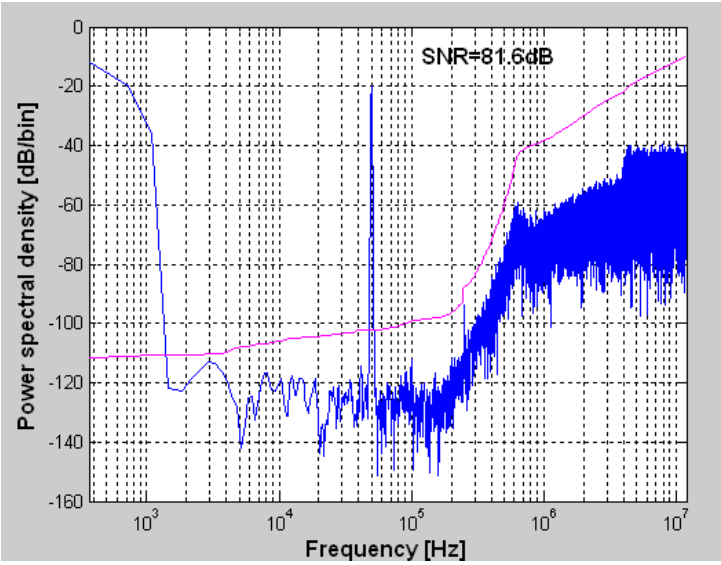

Figure 3.20: Measured result @ input frequency of 50kHz.

3.6 Experimental Results for Second Revision

The layout floorplan is shown in Figure 3.21. The main advantage is increasing isolation between analog portion and digital portion. The phase generator and bootstrapped switches are located at the top side; however, the OTAs are placed at the

bottom side. Compared to the floorplan in the first silicon, the sensitive analog portion is no longer surrounded by noisy circuitry. The drawback is the compromised symmetry between positive portion and negative portion, especially for those interconnections between integrators. Another shortcoming is long switch array, which will impact the chip dimension.

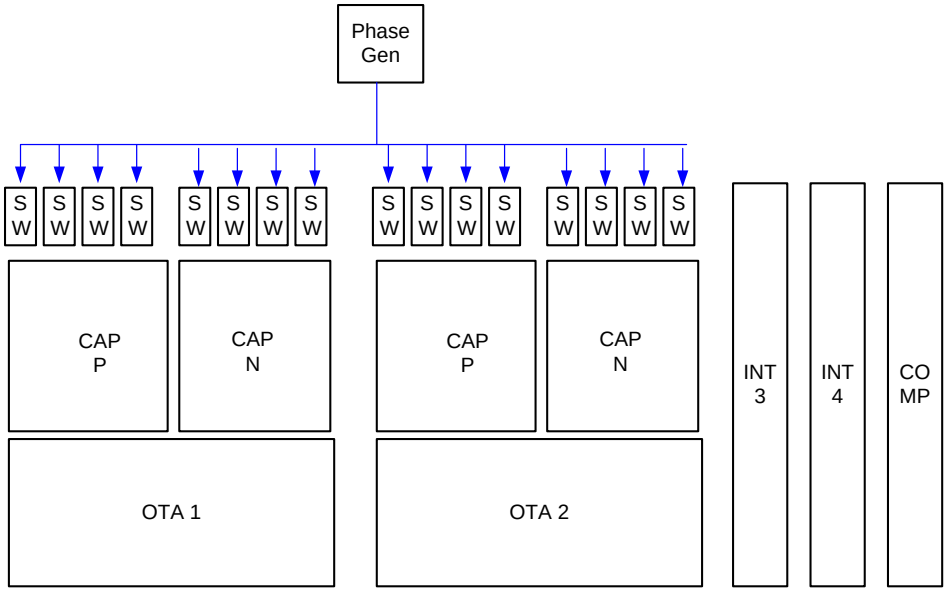

Figure 3.21: Layout floorplan for second revision.

The layout view and pin assignment are shown in Figure 3.22 and Figure 3.23. The test chip is fabricated in a 0.13-μm CMOS technology with MIM capacitor. The die photo is shown in Figure 3.25. Those four integrators are laid out from left to right. The phase generator sits at top side and the quantizer at right side. This arrangement reduces the coupling from digital portion to sensitive analog circuits. The die size is 3 mm x 1.8 mm including the bonding pad and on-chip decoupling capacitors.

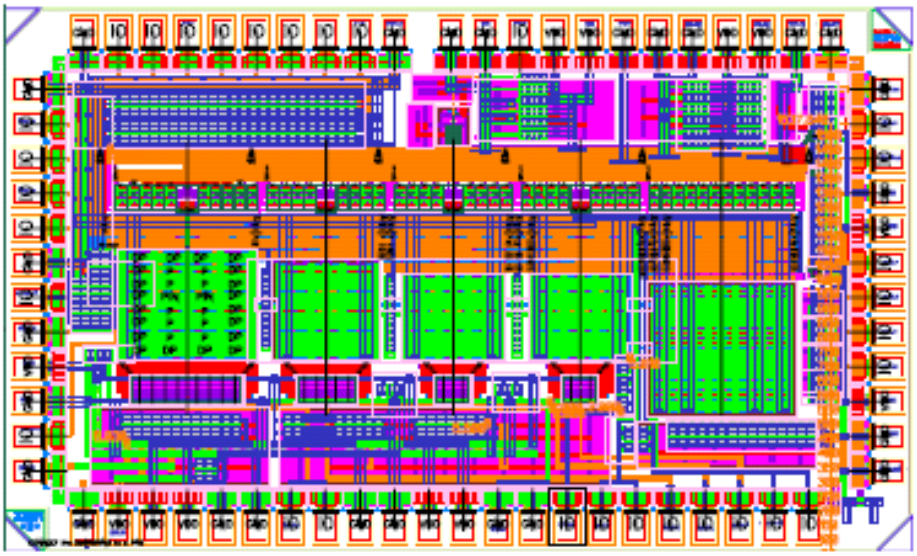

Figure 3.22: The layout view for second revision.

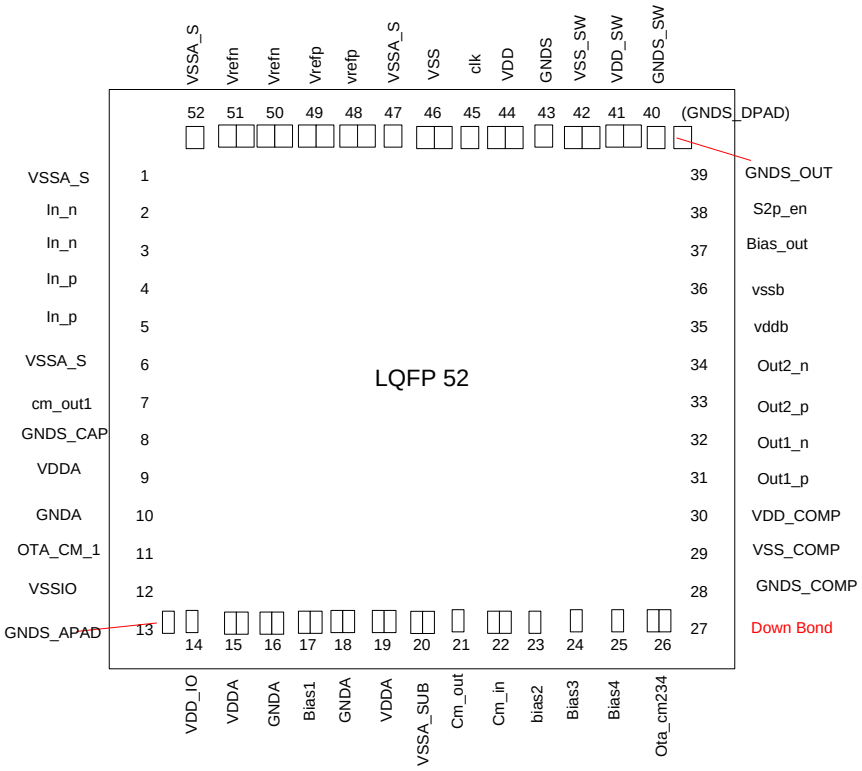

Figure 3.23: The pin assignment for second revision.

The chip is tested in a LQFP package. The fully differential input signal is generated by an ultra low distortion function generator - SRS DS360. The 160 MHz clock source is provided from a pulse generator - Agilent 8133A. Separate power supplies

are used for digital and analog circuits. Some common mode voltage and biasing current are generated on the PCB board. The PCB design is shown in Figure 3.24.

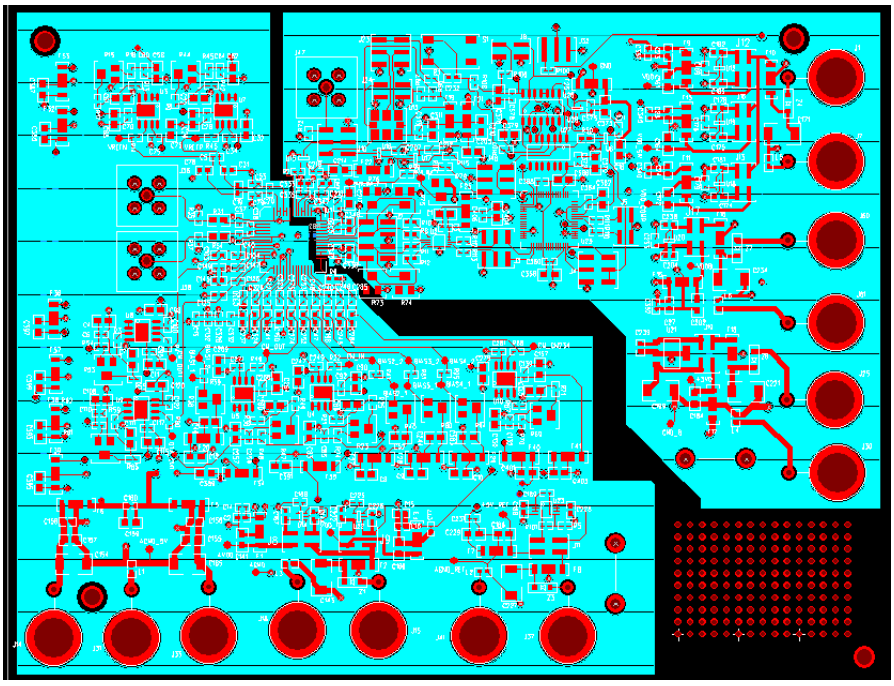

Figure 3.24: The PCB design for second revision.

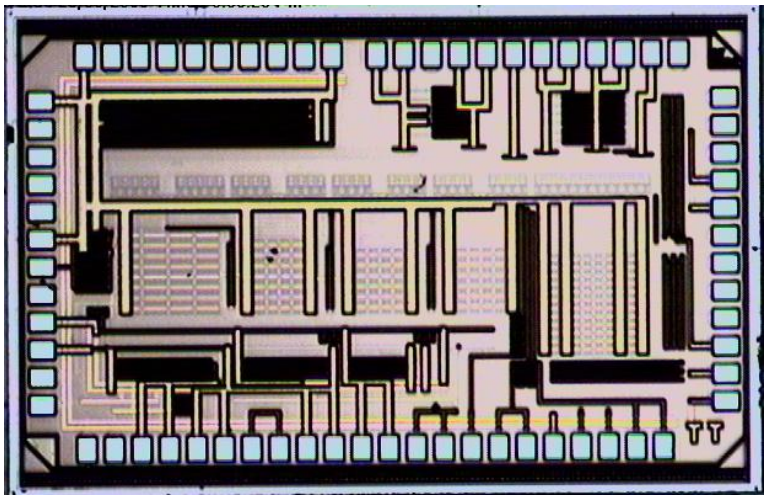

Figure 3.25: The Die photo for second revision.

The measured output spectrum with the peak SNDR of 78.3 dB is plotted in Figure 3.26, with input frequency of 50 kHz. As observed, the second and third harmonics of the output signal is only slightly above the thermal noise floor, which indicates high

linearity is achieved with this input feedforward topology, with the supply voltage of only 1.0 V.

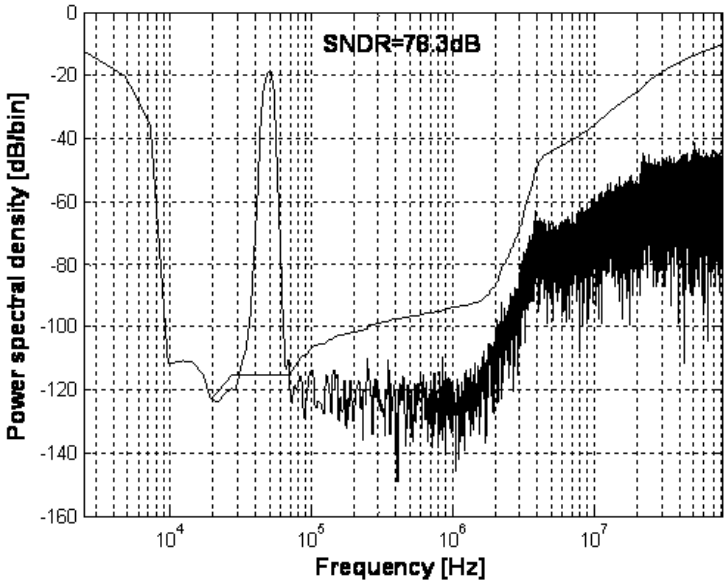

Figure 3.26: Measured output spectrum with Fin = 50 kHz.

Figure 3.27 shows the measured SNR and SNDR versus the normalized input signal amplitude. The dynamic range of 82.5 dB is achieved. With careful design and layout, the ADC performance is not degraded by the high-speed operation.

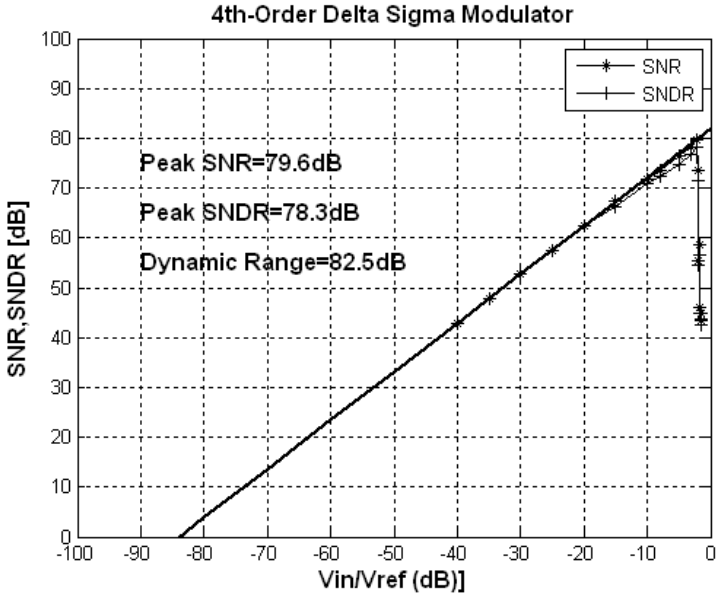

Figure 3.27: SNR and SNDR curve vs. input amplitude.

The measured power consumption is 23 mW, in which 20 mW is consumed by the analog portion and 3 mW by the digital portion. For comparison with others' work, the figure-of-merit (FOM) is defined as

$$FOM = \frac{p}{2 * BW * 2^{ENOB}}, \quad (3.4)$$

where P is the total power consumption, BW is the input bandwidth, ENOB is the effective number of bits, which can be calculated from the peak SNDR as

$$ENOB = \frac{SNDR - 1.76}{6.02}. \quad (3.5)$$

The achieved FOM is 1.35 pJ/conversion. The slightly high power consumption is partly due to the overdesign.

The measured performance is summarized in Table 3.2. The comparison with others' work is shown in Table 3.3. One additional thing worthy to mention, which is missing from the table, is the design complexity. With the input feedforward topology, the implementation is much easier, compared with [11] and [16]. Simple and robust design for the analog building blocks makes this approach more repeatable during mass production.

Table 3.2: Summarization for performance

Conversion Rate	2.5 Msps
Sampling Frequency	160 MHz
OSR	64
Dynamic Range	82.5 dB
Peak SNR	79.6 dB
Peak SNDR	78.3 dB
Max Input Amplitude	0.7 V Differential

Reference Voltage	1.0 V
Power Supply	1.0 V
Power Consumption	23 mW
FOM	1.35 pJ/conversion
Process	0.13 μm CMOS
Total Area	3 mm X 1.8 mm

Table 3.3: Performance comparison

	This work	Pio, 2004 [8]	Nam, 2005 [11]	Cao, 2007 [16]
Supply (V)	1.0	1.8	1.2	2.4
DR (dB)	82.5	84	96	84
BW (MHz)	1.25	12.5	1.25	1.25
Power (mW)	23	200	87	14
FOM (pJ/Conv)	1.35	2.46	1.51	1.22
Technology	0.13 μm	0.18 μm	0.25 μm	0.25 μm

3.7 Conclusions

In this paper, the trade-offs in designing high-speed, low-voltage, low-power Delta-Sigma ADC in deep sub-micron CMOS are discussed. By introducing the input feedforward topology to the Delta-Sigma modulator, some unique advantages are achieved. Main features of the input feedforward Delta-Sigma modulator topology are the unity signal transfer function and low internal swings, which are desirable for

deep sub-micron CMOS designs. A test chip implemented with a 0.13-μm CMOS technology is presented. The circuit level implementation is simple and robust, benefited from the advanced architecture design. The measurement results demonstrate that the proposed input feedforward Delta-Sigma modulator topology is an ideal candidate for high-speed, low-voltage, low-power Delta-Sigma modulator designs in deep submicron CMOS technologies.

CHAPTER 4 A 1-V, 85-DB, 25-MS/S, MULTI-BIT DELTA-SIGMA MODULATOR

4.1 Introduction

Analog-to-digital converter (ADC) is a critical component in modern digital communication systems. The specification of ADC limits the performance of the whole system.

The data rate of digital communication is continuously increasing. However, the available channel bandwidth does not increase proportionally, especially for digital subscriber loop (DSL). More elaborate modulation schemes (for example QAM) are adopted to achieve high data rate. This demands high dynamic range from ADC. For example, the data modems in DSL system require ADC with 13–14 bit accuracy. Interference immunity is another reason for high dynamic range.

Meanwhile, the demanding on ADC bandwidth is also increasing. In [44], a 14 bit 2.5 MS/s Delta-Sigma ADC is implemented for ADSL system. The VDSL standard, makes 12 MHz signal bandwidth available for modem applications with a limited 1.5 km reach along the subscriber loop [45]. It requires the effective conversion rate of 25 MS/s.

In [8], a 25 MS/s, 14 bit Delta-Sigma modulation is implemented. It employed feedforward topology to reduce the signal swing at integrator outputs. However, it requires an OTA with DC gain of 90 dB and GBW of 1.9 GHz. Among the total power consumption of 200 mW, 26% is spent on the first OTA with complex gain boosting scheme.

In this work, a 25 MS/s, multi-bit, discrete-time Delta-Sigma modulator with 85 dB dynamic range is presented. It employs input feedforward topology to relax the specification from the building OTA. With input feedforward topology, the integrator output is reduced further, compared with the normal feedforward topology. Meanwhile, the OTA's DC gain of only 40 dB is required to achieve the ADC's dynamic range of 85 dB. This reduces the power consumption significantly.

To increase the conversion rate from Delta-Sigma modulator, the system clock for oversampling can be increased. However, the requirement on jitter performance becomes much higher. Another option is to reduce the over-sampling ratio and use multi-bit internal ADC. In this work, a 5^{th}-order loop filter with 4-bit quantizer is proposed to achieve 85 dB dynamic range, with the oversampling ratio of 8 and clock rate of 200 MHz. The estimated power consumption is 50 mW, with 1.0 V supply voltage.

The focus of this work is on the architecture design, without experimental results. The detailed design procedures (including MATLAB scripts) are presented, which can be used as a reference for future research on this topic.

4.2 Design Considerations

4.2.1 Oversampling Ratio and Filter Type

To achieve the conversion rate of 25 MS/s, high oversampling clock is preferred. However, high frequency clock is difficult to manage during circuit implementation and silicon evaluation. For the 0.13 μm technology, the clock speed of 200 MHz is a feasible starting point for the architecture design. The oversample ratio (OSR) is calculated as 8.

The Delta-Sigma modulator can be implemented in either discrete time or continuous time. The jitter sensitivity is an important factor for this decision. For the sampling systems, the uncertainty of acquisition instant caused by the clock jitter results in some error in the acquired amplitude, which degrades the ADC's dynamic range. For the discrete-time modulator, the sampling error caused by clock jitter only undergoes the modulator STF (signal transfer function) before reaching the output. The upper limit of SNR can be calculated as

$$SNR < \frac{OSR}{8\pi^2 f_B^{\,2} * \sigma_T^{\,2}}, \qquad (4.1)$$

where, *OSR* is the oversampling ratio, f_B is the signal bandwidth, σ_T is standard deviation of clock jitter. With the *OSR* of 8, the signal bandwidth of 12.5 MHz, the calculated jitter requirement is 0.9 ps for the SNR of 90 dB.

For the continuous time modulator, the sampling operation is located at the output of loop filter. The fundamental of Delta-Sigma modulator is to shape the quantization noise from low frequency to higher band, which makes the signal at the output of loop filter varying much faster than the modulator input. This indicates higher jitter sensitivity for the continuous time modulator. In [46], the SNR upper limit is calculated as

$$SNR < \frac{c^2 m^2 OSR}{8\pi^2 f_s^{\,2} * \sigma_T^{\,2}}, \qquad (4.2)$$

where, f_s is the sampling frequency, *c* is the DAC duty cycle, and *m* is the loop stability coefficient. With *c* = 0.5 and *m* = -5 DBFS, the required jitter is 0.09 ps with equivalent specification as discrete-time one.

With relaxed requirement on the clock jitter, the discrete-time design is selected for this work.

4.2.2 Multi-bit Quantizer and Filter Order

With the OSR fixed at 8, either high order loop filter or higher resolution from internal ADC is required. The higher order for the loop filter, the more chance to be unstable. However, the multi-bit quantizer inside the modulator can relax the stability issue. The most significant drawback of multi-bit quantizer is to eliminate the inherit linearity from the single-bit feedback DAC. This issue can be tackled by the dynamic element matching.

To decide the number of order (L) for the loop filter and number of bits (B) for the internal ADC, the achievable SNR with ideal noise shaping is shown in Figure 4.1. To achieve the dynamic range of 85 dB, L=5 and B=4 is a good choice, with considering the additional contribution from zero-optimization as the margin.

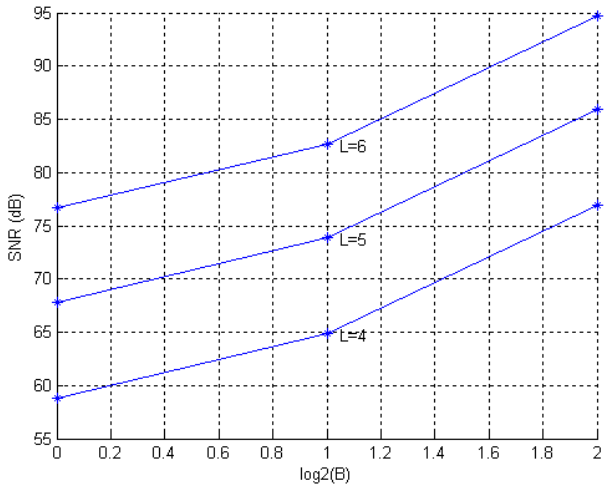

Figure 4.1: The achievable SNR with different L and B.

4.2.3 Zero Optimization

In [3], the technique of zero optimization is described. By shifting the NTF zeros from dc to an optimized location, the SNR can be improved significantly. The optimal zero location is calculated by equating the partial derivatives of NTF integral to zero. The

SNR improvement vs. zero location is listed in Table 4.1. With *L*=5, the potential SNR improvement from zero optimization is 18 dB.

Table 4.1: Zero optimization for minimum in-band noise.

L	Zero location, normalized to 2*pi*f_B	SNR improvement
1	0	0 dB
2	$\pm 1/(\sqrt{3})$	3.5 dB
3	$0,\pm\sqrt{3/5}$	8 dB
4	$\pm\sqrt{3/7 \pm \sqrt{(3/7)^2 - 3/35}}$	13 dB
5	$0,\pm\sqrt{5/9 \pm \sqrt{(5/9)^2 - 5/21}}$	18 dB

4.2.4 Input Feedforward Topology

The input feedforward topology [32] is a perfect candidate for Delta-Sigma modulator. Firstly, the signal transfer function of this topology is unity, which is irrelevant to the loop-coefficients. OTA with low DC gain can be adopted without degrading the conversion accuracy. The quantization noise transfer function remains the same as the one of the traditional topology, a single loop topology without feedforward. Secondly, the internal signal swing can be well suppressed by optimizing the loop coefficients. Besides, there is only one feedback signal to the first integrator, which simplifies the circuit implementation compared to the traditional topology.

For deep submicron process, the intrinsic DC gain from single transistor is becoming lower due to short channel effect. To use single-stage amplifier for low power consumption, the input feedforward topology is adopted.

4.2.5 Cascade or Non-cascade Topology

It is known the cascaded loop filter can be used to realize high order Delta-Sigma modulator with relaxed requirement on the stability. However, good matching is required between the cascaded loop filers. This leads to high DC gain from the building OTA, which is contradictory with the low DC gain requirement benefited from the input feedforward topology.

To take the advantage of deep submicron process, a single loop topology, instead of cascaded one, is used for this work.

4.3 Architecture Design

4.3.1 Loop Filter

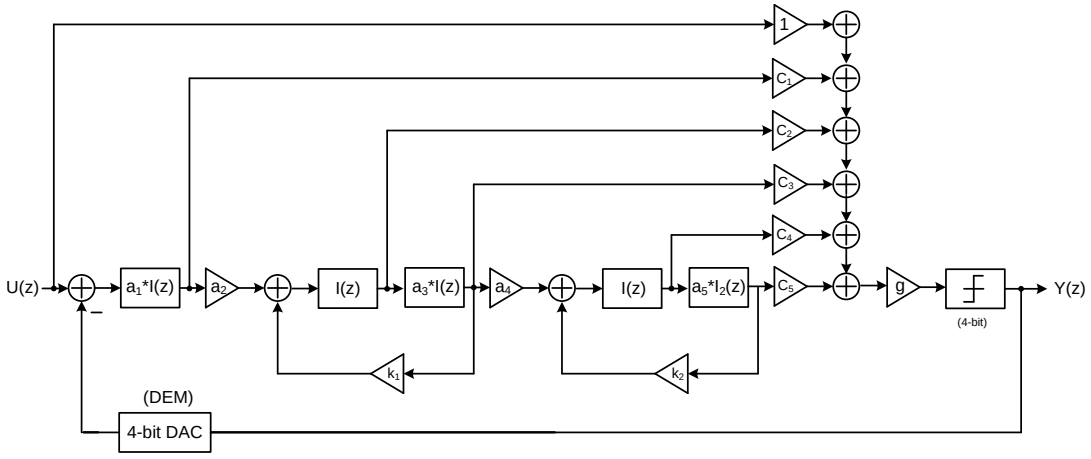

Figure 4.2: The schematic for loop filter.

The schematic of the loop filter is shown in Figure 4.2, in which $I(z)$ and $I_2(z)$ are defined as

$$I(z)=\frac{z^{-1}}{1-z^{-1}};I_2(z)=\frac{1}{1-z^{-1}}. \qquad (4.3)$$

$I(z)$ is the z-domain transfer function for delayed switched capacitor integrator, and $I_2(z)$ is the z-domain transfer function for delay-free switched capacitor integrator.

The 5^{th}-order loop filter contains 5 integrators, whose output are feed and summed at the input of internal ADC. The modulator input is also feed with gain of 1. A pre-amplifier with gain of *g* is inserted to fully utilize the dynamic range of the ADC. A 4-bit ADC converts the amplified sum into digital format, as the modulator output. The negative feedback is completed by a 4-bit DAC, equipped with dynamic element matching technique for high linearity. With the filter order of 5, two pairs of zeros are optimized with the local feedback using the coefficients of k_1 and k_2.

4.3.2 Filter Coefficients

The loop filter coefficients can be obtained using a classical filter function such as the inverse Chebyshev filter for the NTF. The Delta-Sigma toolbox [47] based on CLANS method can be used to achieve the best compromise between stable input range and total integrated in-band noise. The MATLAB function of *clans* is defined as

$$ntf = clans(order = 4, OSR = 64, Q = 5, r = 0.95, opt = 0), \quad (4.4)$$

where, *clans* is a MATLAB function to synthesize a noise transfer function (NTF) for a low-pass delta-sigma modulator using the CLANS (Closed-loop analysis of noise-shaper) methodology [48]. The parameters of *order* and *OSR* are for the filter order and oversampling ratio. *Q* is the maximum number of quantization levels used by the fed-back quantization noise. The parameter of *r* is the maximum radius for the NTF poles and *opt* is to enable/disable zero optimization.

The parameter of *Q* is the most critical parameter. The larger *Q*, the higher achievable SNR. However, the loop is more prone to un-stability with larger *Q*. An iterative loop is implemented in MATLAB to find the optimal value of *Q*. The result is shown in Figure 4.3, from which *Q*=7.22 is chosen. Notes: During simulation, if the un-stable

condition is detected, the simulation is terminated in advance to save simulation time and the output SNR is set to 0dB. Also, it is obvious the loop becomes unstable with Q close to 8. With Q=7.22, some design margin is added.

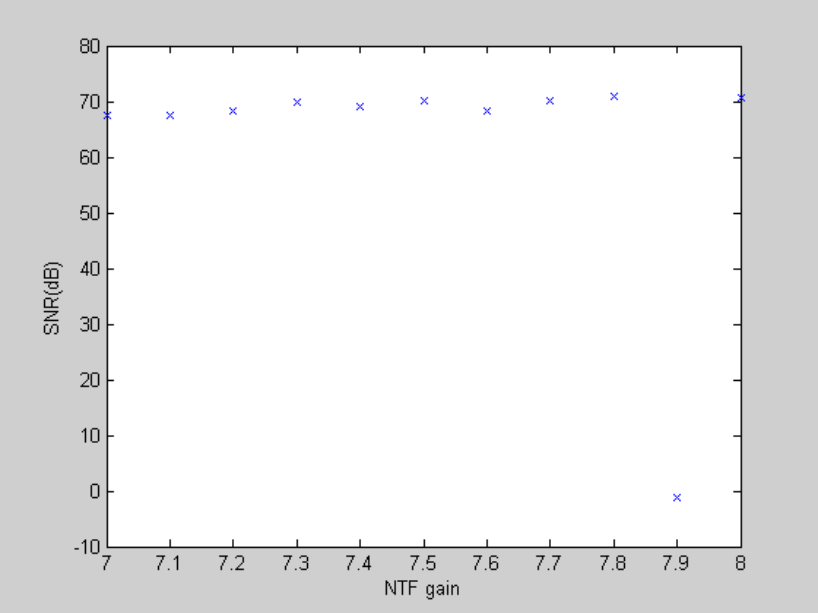

Figure 4.3: The optimal Q parameter for NTF filter.

To relax the design difficulties, the processing of zero optimization is treated separately. The MATLAB program is listed here for future reference.

```
H= clans(5,8,7.22,.9,0);
H.z{1}(2) = 1; H.z{1}(3) = 1; H.z{1}(4) = 1; H.z{1}(5) = 1;
[num, den] = zp2tf(H.z{1},H.p{1},H.k);
syms z; num_s = poly2sym(num, z); den_s = poly2sym(den, z);
H_s = num_s / den_s; I_s = z^-1/(1-z^-1);
I_inv_s = finverse(I_s); L_s = 1/H_s - 1;
L_s_c = compose(L_s,I_inv_s); L_s_c_exp = expand(L_s_c);
coef_hl = sym2poly(L_s_c_exp);
c1=2; c2=2; c3=2; c4=1; c5=1;
a1 = coef_hl(5)/c1; a2 = coef_hl(4)/(a1*c2); a3 = coef_hl(3)/(a1*a2*c3);
```

*a4 = coef_hl(2)/(a1*a2*a3*c4); a5 = coef_hl(1)/(a1*a2*a3*a4*c5);*

The program starts from the *clans* function, from which the NTF filter parameters are returned. After forcing all zeros to DC, some symbolic calculation is performed to map the filter parameters to the input feedforward topology. The feedforward parameter (c1,…,c5) is chosen to minimize the signal swing at integrators' output.

The zero optimization is achieved using another MATLAB program.

H_zero_new = clans(5,8,7.22,.9,1);

zero_i = abs(imag(H_zero_new.z{1}(2)));

*H_zero_new.z{1}(2) = 1 - i*zero_i*zero_factor;*

*H_zero_new.z{1}(3) = 1 + i*zero_i*zero_factor;*

*zz_2 = H_zero_new.z{1}(2) * H_zero_new.z{1}(3);*

zz_1 = H_zero_new.z{1}(4) + H_zero_new.z{1}(5);

k1 = (1- zz_2)/a3; k2 = (zz_1 - 2)/a5;

in which, *zero_factor* is set as 1.06. It is derived from multiple transient simulations. The calculated filter coefficient is

[a1 a2 a3 a4 a5] = [1.5634 1.2589 0.6604 0.6608 0.0870]

[c1 c2 c3 c4 c5] = [2 2 2 1 1]

[k1 k2] = [0.0750 1.4407]

The filter coefficients are rounded to

[a1 a2 a3 a4 a5] = [16/10 17/13 2/3 11/16 1/7]

[c1 c2 c3 c4 c5] = [2 2 2 1 1]

[k1 k2] = [1/13 14/16]

The output spectrum is plotted in Figure 4.4, in which the input frequency is 12.5 MHz and input amplitude is 0.7. The archived peak SNR is 88 dB with the OTA gain of 40 dB only. The *kT*/*C* noise is also added at input node. The histogram of

integrators' output is shown in Figure 4.5. The advantage of low output swing from the input feedforward topology is obvious.

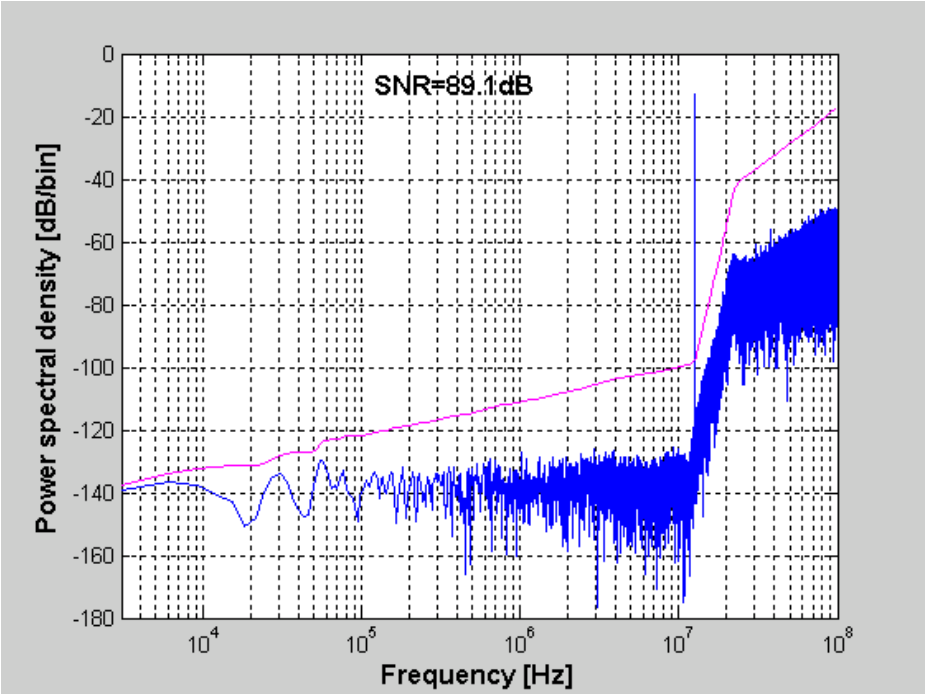

Figure 4.4: The output spectrum from synthesized loop filter.

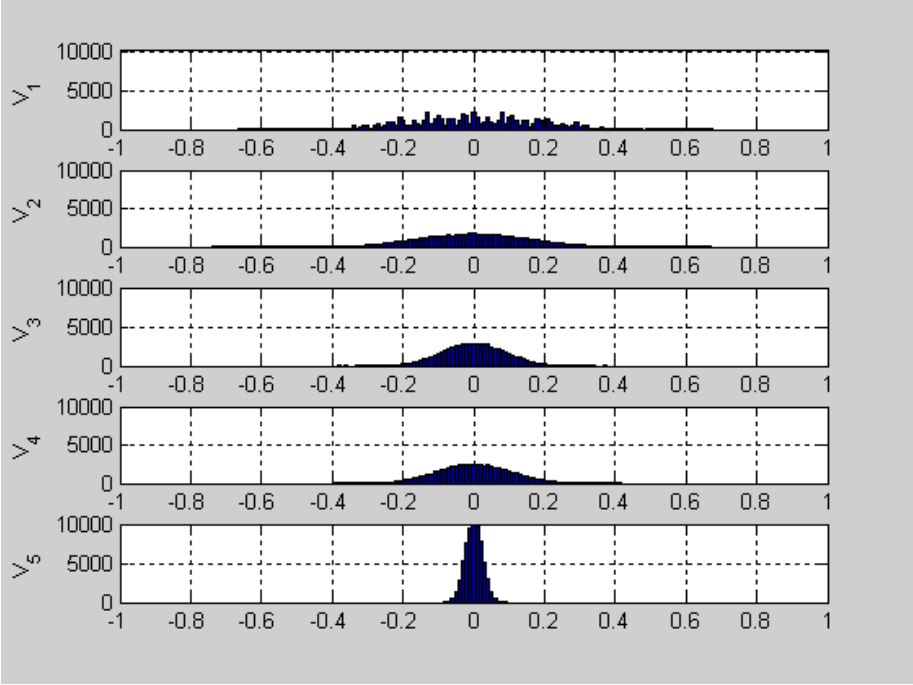

Figure 4.5: The histogram of integrators' output.

The poles and zeros are also plotted in Figure 4.6 to check the stability and zero location. One zero is located at DC, while two pairs of complex zeros are optimized to 6.96 MHz and 11.32 MHz.

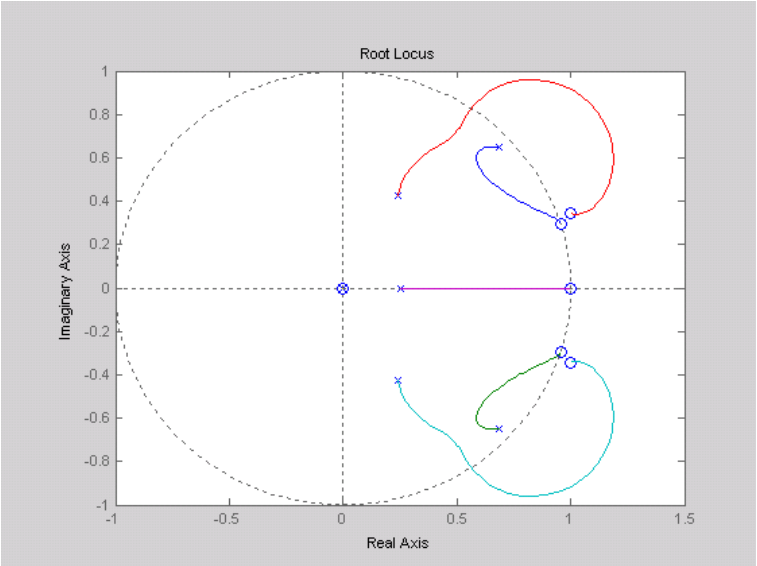

Figure 4.6: The pole and zero for NTF filter.

4.3.3 Sensitivity Check of Filter Coefficients

The sensitivity of filter coefficients is checked by running the MATLAB program for 1000 times. For each run, the filter coefficients are disturbed by some randomly generated error, with standard deviation of 0.5%. The result is shown in Figure 4.7.

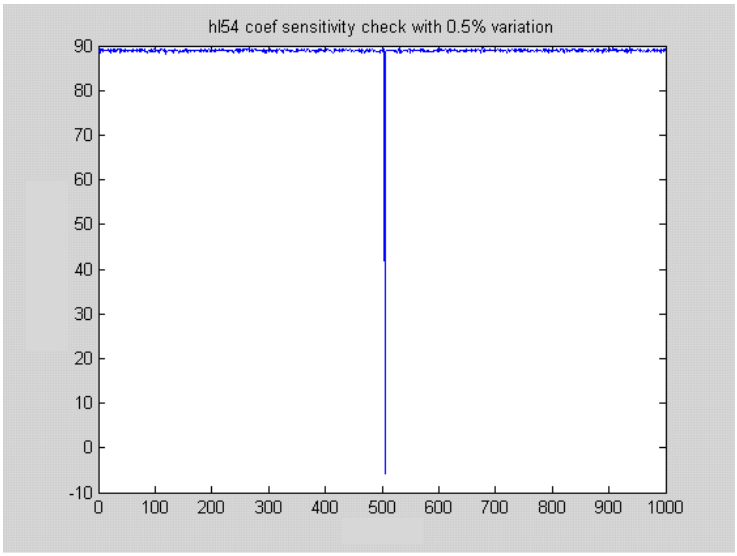

Figure 4.7: Sensitivity check for filter coefficients.

Please note, the input amplitude is fixed at 0.7 and SNR = 0 means unstable. For the unstable cases, the input amplitude has to be reduced slightly.

4.3.4 The Effect of ADC and DAC Nonlinearity

The effect of ADC and DAC nonlinearity is checked, with results shown in Figure 4.8. The difference from ideal transition value (for ADC) and feedback value (for DAC) is defined as offset here. For the contour plot, the axis is the standard deviation from multiple runs. For the DAC, high accuracy is required, which can be realized by DEM. The error from ADC is more relaxed, with 15 mV as the limit. The detailed plots for SNR vs. DAC offset and ADC offset is shown in Figure 4.9 and Figure 4.10.

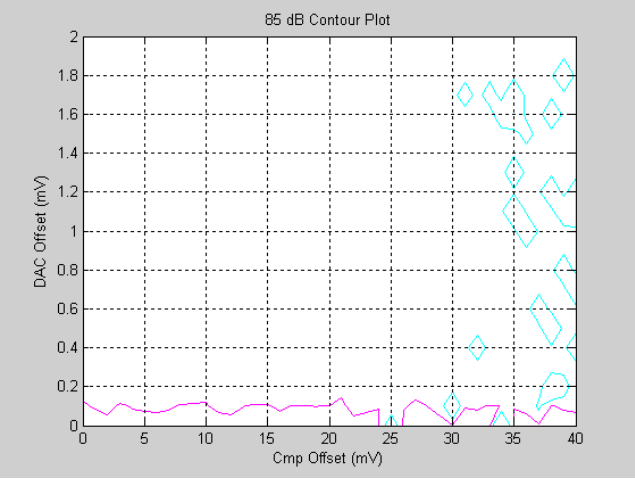

Figure 4.8: Effect of ADC and DAC nonlinearity.

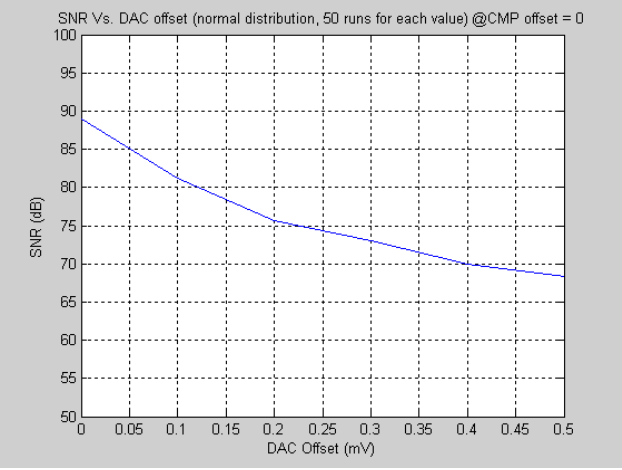

Figure 4.9: The SNR vs. DAC offset with ideal ADC.

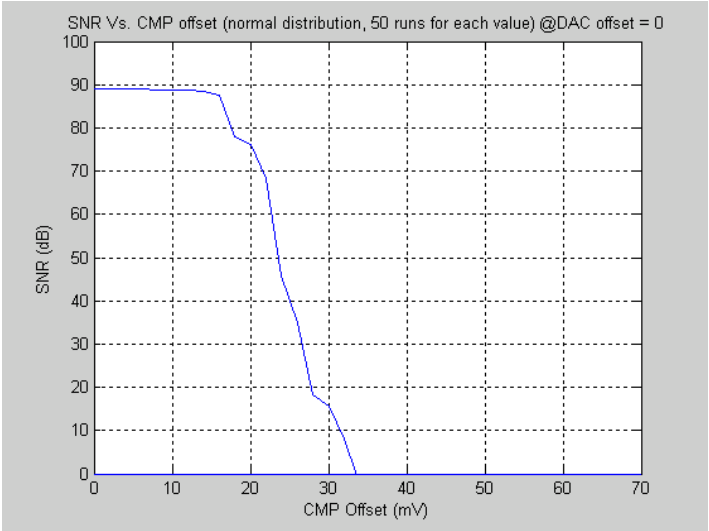

Figure 4.10: The SNR vs. ADC offset with ideal DAC.

4.3.5 Effect of Pre-amplifier Gain

To fully utilize the dynamic range of the internal ADC, a pre-amplifier (*g* in Figure 4.2) is required. The relationship of SNR vs. pre-amplifier gain is shown in Figure 4.11. The usable range of pre-amplifier gain is from 7.5 to 9. Note that the input amplitude is fixed at 0.7 V for this simulation.

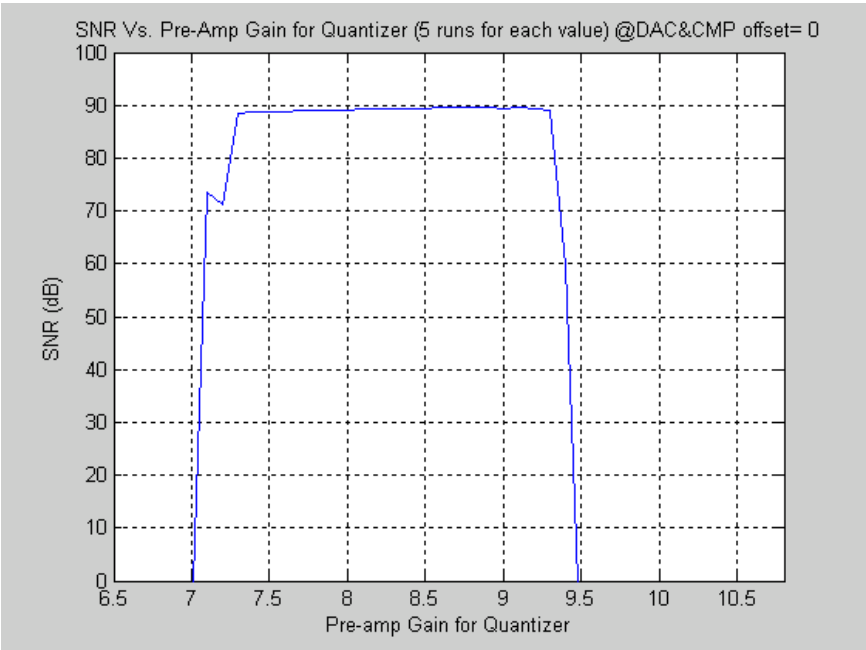

Figure 4.11: The SNR vs. the gain of pre-amplifier.

4.4 Discussion on the Implementation

On the implementation of multi-bit Delta-Sigma modulator with input feedforward, [35] provides detailed discussion and solutions. To relax the timing of feedback path, the input path is duplicated. This leaves more time for ADC, DEM and DAC circuits. For the design of pre-amplifier, [8] provides a good reference. The telescopic OTA with DC gain of about 40 dB can be adopted for low power consumption.

4.5 Conclusions

In this work, the detailed architecture design procedure for an 82 dB, 25 MS/s Delta-Sigma modulator is presented. The MATLAB program is provided for future reference. With input feedforward topology, the modulator can be easily implemented with low supply voltage. The telescopic OTA with DC gain of about 40 dB can be adopted for low power consumption. The reference paper for timing relaxation is also indentified.

CHAPTER 5 A 1-V, 1-MS/S, SAR ADC FOR SENSING SYSTEMS

5.1 Introduction

Portable sensing systems are becoming more popular recently. Capacitive touchscreen controller and handheld ECG monitor are two examples. For both sensing systems, an analog-to-digital converter (ADC) is required to transform some slowly-varying or sampled DC signals into digital format. In other words, it doesn't have to track fast inputs. However, to leave more time for its analog front-end or share it between multiple channels, high conversion rate is required. Low power consumption is critical to extend the battery lifetime.

Successive approximation (SAR) ADC is the optimal choice for these sensing systems. It provides medium resolution (about 10 bit), medium conversion rate (about 1 MS/s) and low power consumption. However, most of recently published SAR ADCs are based on fully differential topology [22] [49] - [53], instead of single-ended one. In those designs, most of power reduction techniques rely on fully differential inputs, which may not be available for some sensing systems. To use differential topology, extra power budget is required for the additional single-end to differential converter. Meanwhile, the differential topology needs almost twice silicon area of single-ended one, because of dual capacitor arrays.

Two examples of single-ended SAR ADC [54] and [29] are based on the topology in Figure 5.1. There are two drawbacks. Firstly, the comparator is required to have same

input range as V_{in}. This is challenging, especially when the input is rail-to-rail. Also, the common-mode dependent offset from the comparator degrades the ADC linearity. Secondly, the parasitic capacitance at V_g node results in gain error, and even nonlinearity error if it has voltage dependency.

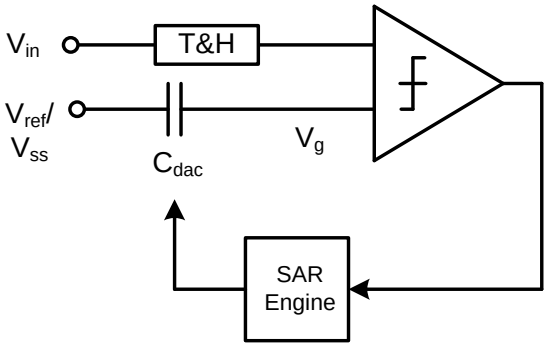

Figure 5.1: Conventional topology for single-ended SAR ADC.

The architecture in Figure 5.2 eliminates these two drawbacks. It is achieved by forcing V_g back to V_{cm} after the convergence of successive approximation, which is the same potential during input tracking. The optimal V_{cm} is at half of reference voltage (V_{ref}), in order to avoid forward biasing the PN junctions inside S_0 during successive approximation. In [55], the reference voltage is used as V_{cm}; a complex charge pump switch is required to prevent leakage due to forward biasing.

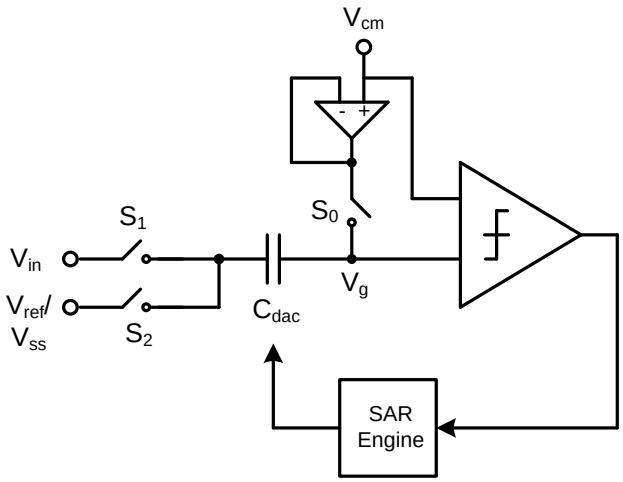

Figure 5.2: Improved topology for singled-ended SAR ADC.

The V_{cm} buffer is power hungry due to large capacitive load from C_{dac}, which is 2~6 pF for 10-bit ADC. Even the V_{cm} buffer is used only during input tracking; it is kept on for the whole conversion, because of long turn-on time compared with short conversion period.

Comparator is another critical block for SAR ADC. Dynamic latched comparator runs fast while consuming little current. However, it is not feasible to use it alone for SAR ADC because of large offset, and even nonlinearity [26] if used in the topology of Figure 5.1. A multi-stage, offset cancelled pre-amplifier is required.

In this work, a single operational transconductance amplifier (OTA) is used as the V_{cm} buffer during input tracking, and reused as the pre-amplifier of latched comparator during successive approximation. The input referred offset error is reduced significantly, without burning additional power for the pre-amplifier. To speed up conversion, the latched comparator is in current-mode style. To reduce power consumption, the OTA is built with a modified CMOS inverter, assisted with an adaptive technique to account for supply, process and temperature variations. Overall, this single-ended SAR ADC works without additional reference generator and biasing circuit, while supporting rail-to-rail input range. Meanwhile, a split capacitor array with dual thermometer decoders is proposed, in order to improve its switching energy efficiency.

5.2 Architecture Design

The proposed single-ended SAR ADC is described in Figure 5.3. It supports rail-to-rail input range, with supply voltage as the reference. Please notes the schematic of OTA is simplified for illustration.

The SAR ADC comprises of a capacitor array, i.e. C_{dac}, a shared OTA, a current-mode latched comparator, a SAR engine and a switch array. The OTA is built with a

modified CMOS inverter (simplified schematic in Figure 5.3), which eliminates the generation of a real V_{cm} voltage, by auto-zeroing between input tracking phase and successive approximation phase. During input tracking, S_1 and S_2 are closed, while S_3 and S_4 are opened. With negative feedback, V_g is forced to a common mode voltage, named as V_{cm1}, which is defined by the relative driving strength of M_n and M_p (in Figure 5.3) inside the CMOS inverter, and the supply voltage. V_{cm1} can be set around $V_{DD}/2$ easily. After settled, the charge stored in C_{dac} is

$$Q_{sample} = (V_{cm1} - V_{in}) * C_{dac}. \qquad (5.1)$$

With S_3 opened, the current flowing through M_n and M_p should be equal. The input sampling is completed by opening S_1, followed by S_2. This clocking scheme eliminates signal-dependent charge injection and clock feedthrough from S_2. The switch error from S_1 only results in minor ADC offset error, due to large C_{dac} value compared with small MOS capacitance inside S_1.

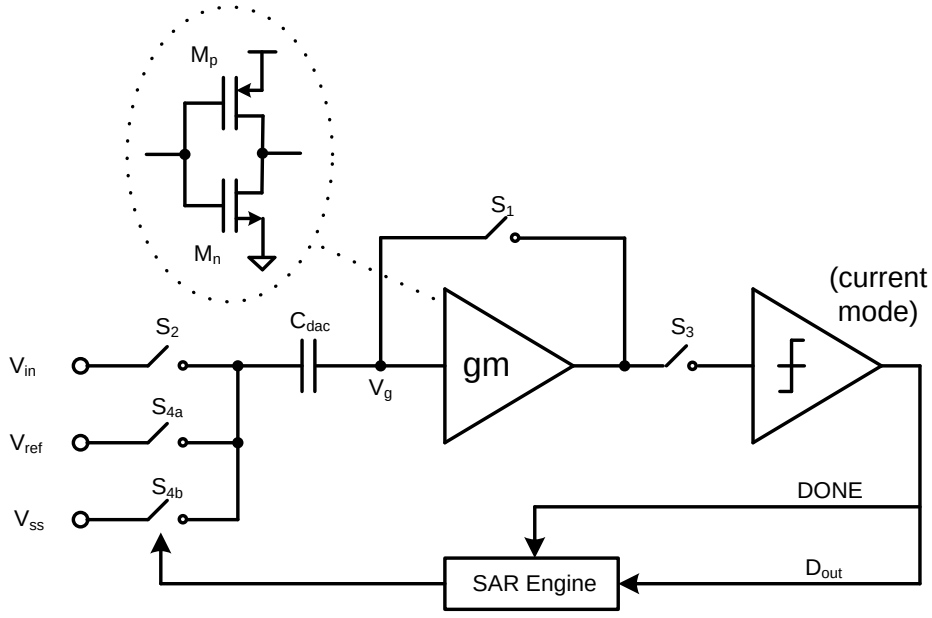

Figure 5.3: The proposed architecture for the SAR ADC.

The successive approximation period starts with closing S_3, and connecting half of C_{dac} to V_{ref}, and another half to V_{ss}. The current-mode comparator performs a

comparison between the current flowing through M_p and that through M_n. If the current through M_p is larger than that through M_n, the comparator result is set as high. The SAR engine and switching array adjusts the voltage divider inside C_{dac} to raise V_g. This reduces the current through M_p and increases the current through M_n. After ten cycles of try-and-clear approximation, the current through M_p is almost equal to that through M_n, with quantization error as the residue. Depending on the implementation of current-mode comparator, the voltage at the OTA output may be different from V_{cm1}, which is the potential during input tracking. This makes V_g deviate slightly from V_{cm1}. The V_g after SAR converging is named as V_{cm2}, and the charge in C_{dac} is

$$Q_{conv} = (V_{cm2} - V_{ref}) * p * C_{dac} + V_{cm2} * (1-p) * C_{dac}, \quad (5.2)$$

where, p is the fraction of C_{dac} connected to V_{ref}. With the law of charge conservation, V_{in} can be simply calculated as

$$V_{in} = p * V_{ref} + (V_{cm2} - V_{cm1}). \quad (5.3)$$

The difference between V_{cm1} and V_{cm2} only causes ADC offset error. With OTA DC gain of A, it can be calculated as

$$V_{cm2} - V_{cm1} = (V_{cm1} - V_o)/A, \quad (5.4)$$

where, V_o is the OTA output after SAR converging. The offset error is ignorable with high enough DC gain (about 60 dB). In this sense, the OTA is reused as the pre-amplifier of the current-mode comparator. Meanwhile, the latch's offset in current mode is attenuated by the OTA's transconductance (gm) before referring back to ADC input.

There are a few benefits to use current-mode comparator, compared with voltage-mode one. Firstly, it eliminates the generation of common mode voltage, because the comparison is performed between zero and the current difference between M_p and M_n.

Secondly, it has low input impedance, which turns the OTA output into a low impedance node. This speeds up the conversion speed and reduces the power consumption indirectly. Lastly, the initial voltage of latch regeneration can be set around $V_{DD}/2$. This reduces comparator dynamic offset due to capacitance mismatch, compared with the dynamic latch [56].

The comparator also generates a "comparison done" signal, which is used by the SAR engine to initiate C_{dac} settling for next bit cycle, right after the comparison decision is made. This increases the settling time for C_{dac} and current-mode comparator. The power consumption is reduced indirectly.

The timing diagram is shown in Figure 5.4. The SAR conversion comprises of 16 clock cycles, in which 5.5 cycles for input tracking, 1.5 cycles for bit 9 (MSB), and 1 cycle for each bit from bit 8 down to bit 0. The allocated number of cycles for input tracking is determined by the trade-off of power consumption between OTA, current mode comparator and digital circuits. Another consideration is OTA's transconductance, which attenuates the offset from the current-mode comparator. For bit 9, 0.5 extra clock cycle is assigned for C_{dac} settling, because the capacitive load on the reference supply is the heaviest among 10 bit cycles.

During the high period of *CLK*, the current-mode comparator senses the current difference between NMOS and PMOS transistors. At the falling edge of *CLK*, the comparator is strobed and starts regeneration. At the rising edge of *DONE* signal, *sar*<5> is set to high while *sar*<6> is cleared. The C_{dac} settling for bit 5 starts immediately. For SAR ADC, critical decision (SAR result close to final value) does not span two consecutive cycles. This property increases C_{dac} settling time for the critical decision, which improves converter accuracy and reduce total power consumption.

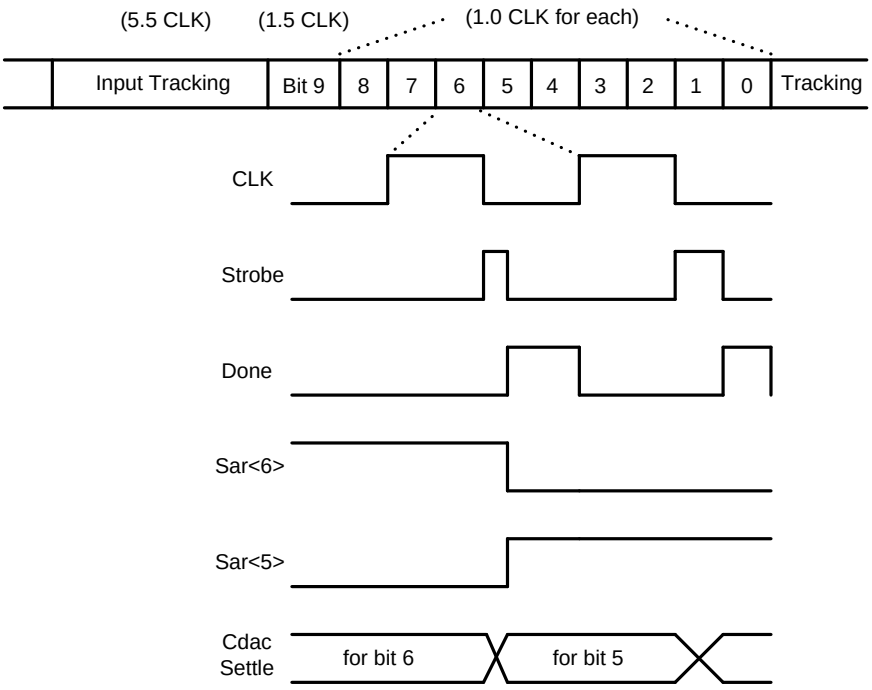

Figure 5.4: The timing diagram.

5.3 The Implementation of SAR ADC

5.3.1 The Capacitor Array

The linearity of SAR ADC is mainly decided by the accuracy of capacitor array, which is shown in Figure 5.5. To reduce total number of capacitors, a split capacitor array [57] is adopted in this work. This topology has two drawbacks. Firstly, to get same accuracy, the size of unit capacitor, C_1 in Figure 5.5, is larger than that in binary capacitor array. However, total area is still smaller, because of much less capacitors included. Secondly, the parasitic capacitor C_p in Figure 5.5, impacts the linearity of SAR ADC. This issue can be fixed by careful shielding and enlarging C_b.

The size of unit capacitor is decided by the mismatch error between all those comprising capacitors. For the technology used, the mismatch error between two unit capacitors (about 80fF) is about 0.4% (2.5 sigma). A MATLAB simulation is implemented to check the linearity of capacitor array. The DNL and INL error are

plot in Figure 5.6 and Figure 5.7. With the size of unit capacitor of 80 fF, the total C_{dac} is about 2.56 pF.

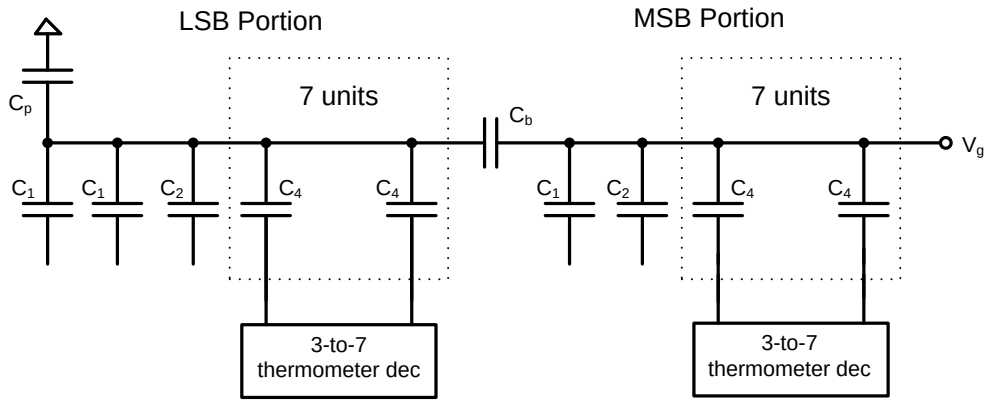

Figure 5.5: The capacitor array, where $C_2 = 2*C_1$, $C_4 = 4*C_1$, $C_b=32/31*C_1$.

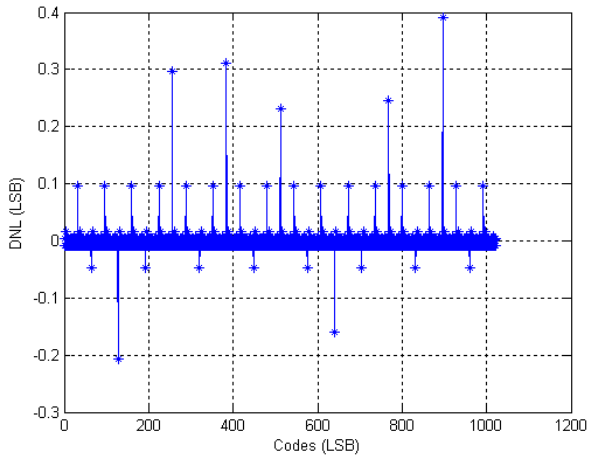

Figure 5.6: The DNL error from MATLAB simulation.

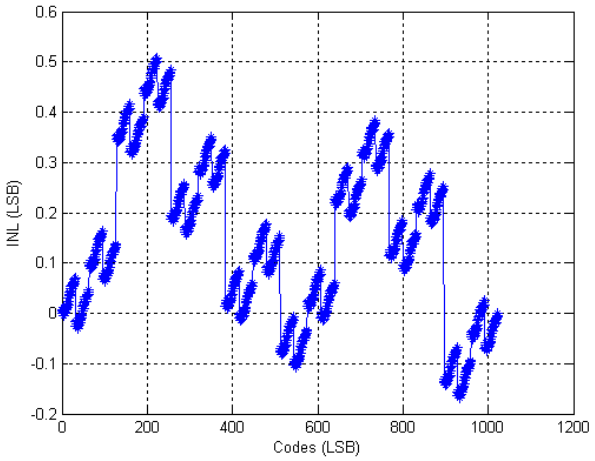

Figure 5.7: The INL error from MATLAB simulation.

To ensure the yield, the same program is executed for 1000 times, with different seeds for the random mismatch errors. The results are shown in Figure 5.8 and Figure 5.9. Please note the maximum DNL/INL errors are the larger one of positive and negative peak value; 95% yield is guaranteed to have max DNL/INL < 1 LSB.

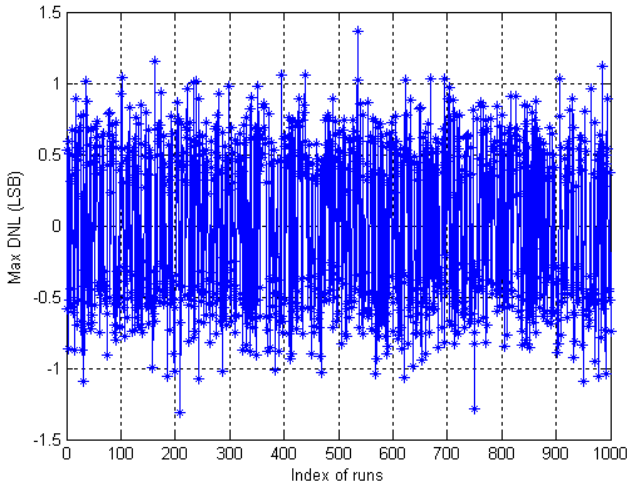

Figure 5.8: The maximum DNL error for 1000 runs.

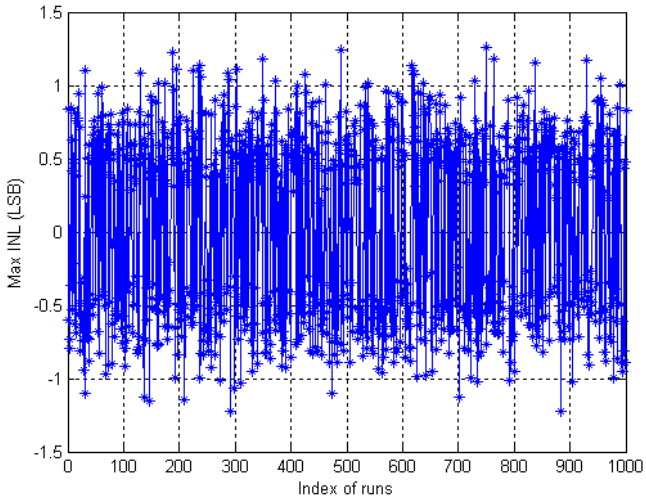

Figure 5.9: The maximum INL error from 1000 runs.

Recently, the switching energy efficiency of capacitor array attracts a lot of attention [26]. In [58], the method of splitting MSB capacitor is proposed; however, its implementation is a bit complex. In this work, a simpler solution with equivalent power saving is proposed. As shown in Figure 5.5, two "3-to-7 thermometer

decoders" are inserted into LSB and MSB portions respectively. Conventionally, thermometer decoder is used in capacitor array to reduce DNL error. However, its capability of reducing switching energy has not being identified. A 2-bit capacitor array is used here for easy illustration, as described in Table 5.1. Notes: *C* is the unit capacitor, *V* is the reference voltage. Please refer to [58] for detailed calculation.

Table 5.1: Switching energy for 2-bit Capacitor array.

Transitions	Binary C_{dac}	Thermometer C_{dac}
2→3	¼*CV^2	¼*CV^2
2→1	¾*CV^2	¼*CV^2

For a 2-bit SAR ADC, to decide the 2nd bit, there are two possible transitions: 2→1 and 2→3. For transition of 2→3, both thermometer capacitor array and binary capacitor array consumes same switching energy ¼*CV^2. However, there is large difference for transition of 2→1. For the binary capacitor array, the transition contains two operations: discharging MSB capacitor to ground and charging LSB capacitor to reference voltage. It consumes less energy if these two operations are completed in two steps [58], compared with that from simultaneous jumps. Even with two-step operation, it consumes ¾*CV^2. For thermometer capacitor array, there is only a single operation for transition 2→1: discharging half of MSB capacitor to ground. It only takes ¼*CV^2 energy. For the detailed calculation of switching energy, please refer to [58]. Overall, the thermometer decoder reduces both DNL error and capacitor array switching energy.

As comparison, the capacitor array switching energy is calculated in MATLAB, for four array topologies: binary capacitor array with one-step switching, binary capacitor array with two-step switching, split capacitor array without thermometer decoder,

split capacitor array with dual thermometer decoder. The comparison result is shown in Figure 5.10 and Table 5.2. Please note the unit capacitor is 1 pF for split capacitor array and 1/8 pF for binary capacitor array.

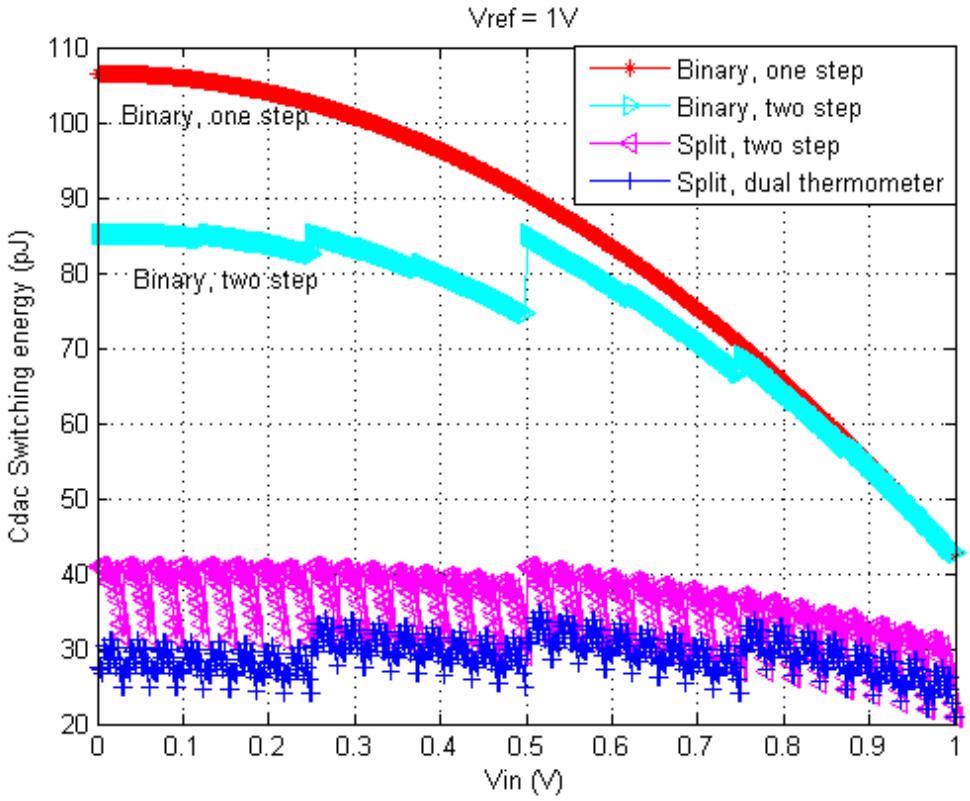

Figure 5.10: Capacitor array switching energy comparison.

Table 5.2: Capacitor array switching energy comparison.

Array type	Average Switching energy (pJ)	Comparison
Binary, one step	85.17	100%
Binary, two step	74.51	87%
Split, two step	35.76	42%
Split, dual thermometer	29.00	34%

The implementation of "binary-to-thermometer" decoder is listed in Table 5.3. During the implementation, extra effort is spent on the delay balance between different paths.

Table 5.3: Implementation of "binary-to-thermometer" decoder.

Output	Logic	Remarks
1	in[2] | in[1] | in[0]	
2	in[2] | in[1]	
3	in[2] | (in[1] & in[0])	Use complex gate.
4	in[2]	Add delay for balance.
5	in[2] & (in[1] | in[0])	Use complex gate.
6	in[2] & in[1]	
7	in[2] & in[1] & in[0]	

To improve the accuracy of the C_{dac}, the technique of dynamic element matching (DEM) is adopted for the MSB portion after its thermometer decoder. Normally, a lot of averaging is required to reduce the environment noise, for the sensing system. Between the multiple samples, the roles of the thermometer elements are rotated in a defined way. This technique is widely used in the multi-bit Delta-Sigma modulator [8]. A 2-bit thermometer capacitor array is used here for illustration. Assume the normalized capacitance of three unit capacitors: 1, $1+e_1$, $1+e_2$, where e_1 and e_2 are the mismatch from the first capacitor. The operation of DEM is illustrated in Table 5.4, in which the roles of those three unit capacitors are rotated in a fixed direction. MATLAB simulation is used to check the effect of DEM. The results from 100 runs with different random seeds for capacitor mismatch error is shown in Figure 5.11 and Figure 5.12. Please note the standard derivation of mismatch error is set to 0.4% as

previously. The improvements on linearity are visible, especially for the INL error. Please note this idea of DEM is implemented to explore new idea only; it won't be in publication.

Table 5.4: Operation of DEM; 2-bit Cdac = {0, C_1, C_1+C_2, C_1+C_2+C_3}.

[C_1 C_2 C_3]	DNL at Code 1	DNL at Code 2	DNL at Code 3
[1 $1+e_1$ $1+e_2$]	0	e_1	e_2
[$1+e_2$ 1 $1+e_1$]	e_2	0	e_1
[$1+e_1$ $1+e_2$ 1]	e_1	e_2	0
Averaged from 3 runs	$(e_1+ e_2)/3$	$(e_1+ e_2)/3$	$(e_1+e_2)/3$

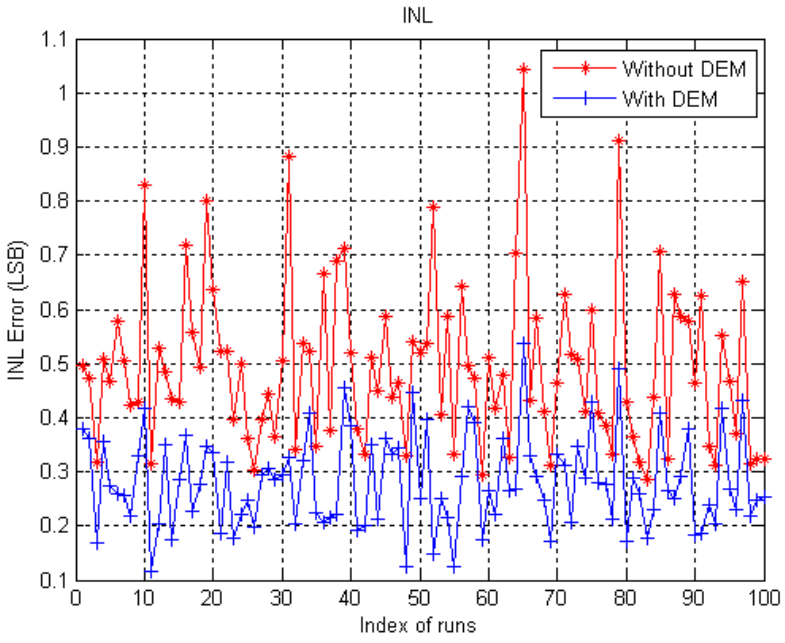

Figure 5.11: The improvements on INL error from DEM.

The capacitor array is implemented with metal finger capacitor. To reduce parasitic capacitance, C_p (to ground) in Figure 5.5, polysilicon and Metal 4 are used as

shielding mask, which is connected to bottom plate of C_{dac}. Only metal 1~3 are used for finger capacitor due to process limitation.

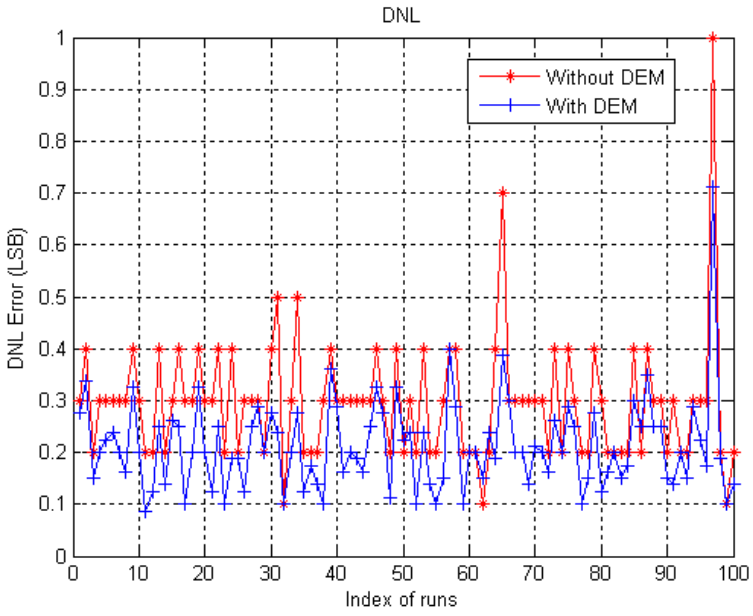

Figure 5.12: The improvements on DNL error from DEM.

5.3.2 Operational Transconductance Amplifier (OTA)

The OTA is the most critical design blocks for this SAR ADC. Its transconductance (gm) decides the time constant (*TC*) during input tracking by

$$TC = C_{dac} / gm. \qquad (5.5)$$

For high-speed SAR ADC, the input tracking is completed in a short time. The OTA's power efficiency directly determines the figure-of-merit (*FOM*) of whole ADC.

To drive a large capacitive load, a single-stage OTA has highest power efficiency, in which the loaded capacitor is used for compensation implicitly. However, single-stage OTA is not suitable for tracking of high frequency signal, because the OTA gain around Nyquist frequency is too low to maintain a stable common mode voltage

under fast-varying input. This is not an issue for the targeted sensing systems, with slowly varying or sampled DC signals as input.

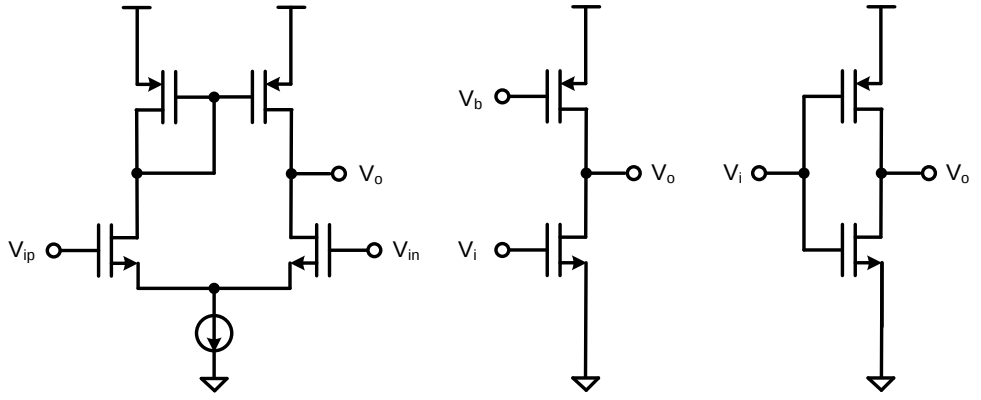

Figure 5.13: Three topologies for single-stage OTA.

Figure 5.13 lists three single-stage OTA topologies. For comparison, the power efficiency is defined as

$$E = gm / I , \qquad (5.6)$$

where I is total static current. The power efficiency of common-source amplifier in Figure 5.13B is normalized as 1. For the differential pair in Figure 5.13A, two current branches are included. However, only one of them contributes the effective transconductance; so the power efficiency is halved. For the CMOS inverter in Figure 5.13C, there is only one current branch, which is used by both PMOS and NMOS to double transconductance and power efficiency.

Meanwhile, the CMOS inverter has best slew behavior. Dependent on input polarity, this amplifier can sink or source large current in short time. However, for common-source amplifier, the positive slew is limited by the PMOS active load. In the differential pair, both positive and negative slew rate are limited by the same tail current.

During input tracking, large transconductance and slew rate shorten the settling time. For high power efficiency, CMOS inverter is selected for this work. Also, it enables the possibility to eliminate additional reference generator and biasing circuits. However, it has large g_m variation under different process and temperature. This can be easily solved by adding enough margins. However, it takes away some power saving from using CMOS inverter as OTA. Although CMOS inverter consumes less power than other alternatives with additional reference and biasing requirements, one adaptive method to tackle g_m variation is proposed in Figure 5.14.

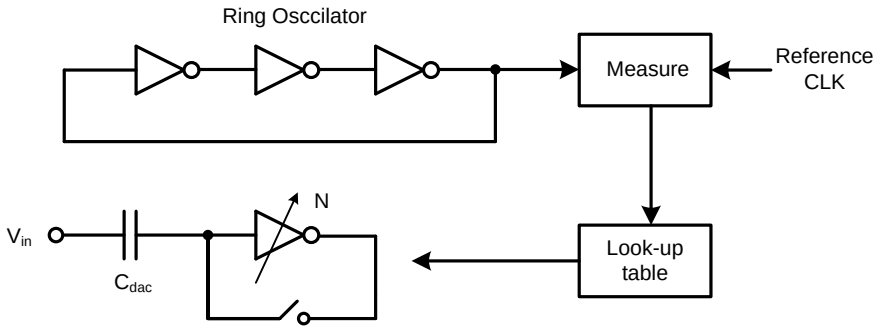

Figure 5.14: The adaptive technique for the CMOS inverter.

To enable the adaptive technique, the CMOS inverter (or OTA) is split into *N* units. The same unit is used to build a ring oscillator, whose output frequency is measured with a reference clock. Based on the oscillation frequency, the OTA is configured with a look-up-table. Fast oscillation frequency indicates large OTA transconductance. To reduce design complexity, *N* is set as 4 and the coarse look-up-table is implemented off-chip for this work. The ring oscillator is disabled by default, and can be waked up periodically (in seconds, dependent on its application) for trimming.

To check the feasibility of the adaptive scheme, some spectre simulations are executed on the transconductance (g_m) of OTA and oscillation frequency of ring oscillator, under different temperature and process variations. The variation of trans-

conductance is shown in Figure 5.15, while the variation of oscillation frequency is shown in Figure 5.16. From the trends of both plots, it shows the correlation between these two parameters can be used to adjust the number of OTA units.

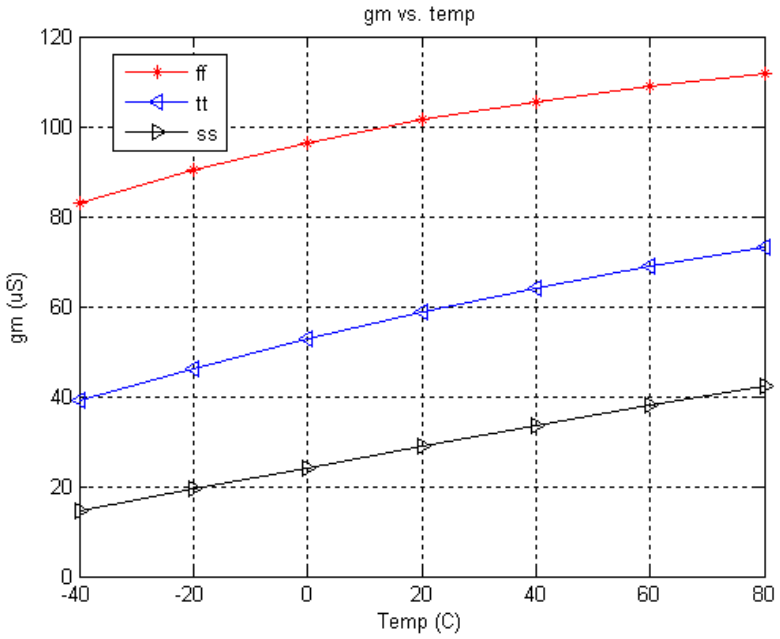

Figure 5.15: The variation of gm vs. temperature and process variation.

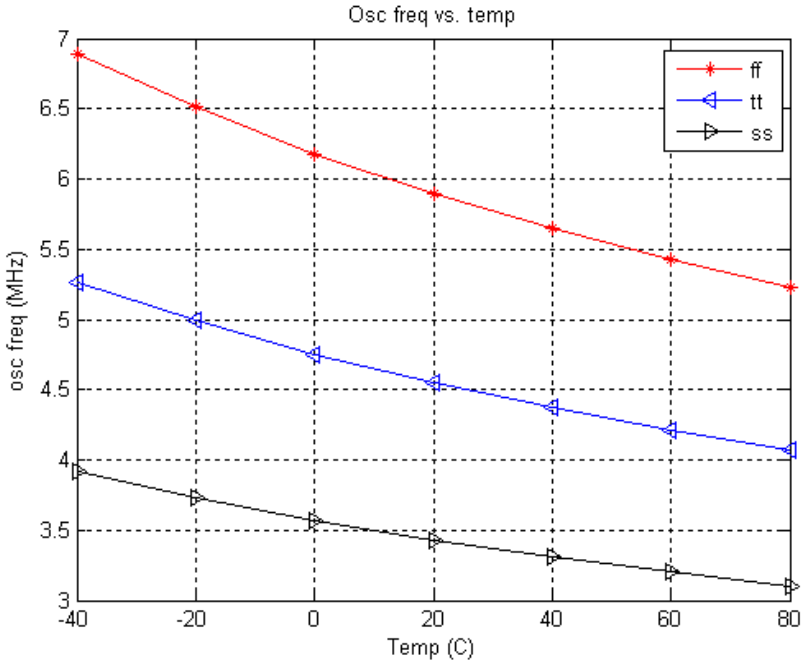

Figure 5.16: The ring oscillator frequency vs. temp and process variation.

As mentioned in Section II, DC gain of 60 dB is enough to maintain a stable common mode and to get rid of the offset error due to the difference between V_{cm1} and V_{cm2}. For 0.13 μm CMOS technology, the DC gain of simple CMOS inverter is only 30 dB. Cascode is mostly conventional method to increase DC gain. However, the additional biasing circuit increases power consumption. In this work, one simplified cascode method is proposed in Figure 5.17.

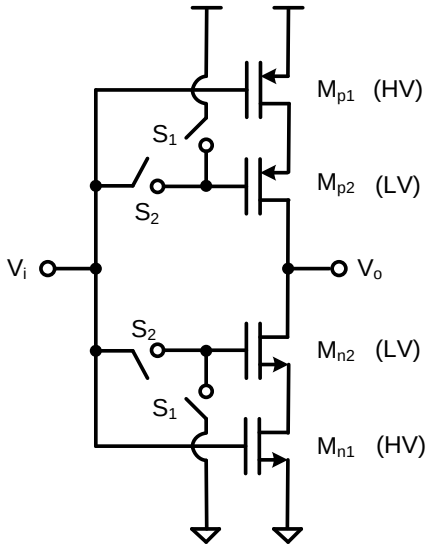

Figure 5.17: The detailed schematic for OTA.

In the modified CMOS inverter, the gates of cascode devices are shorted to OTA input, in order to save the power for biasing generation. For the CMOS technology used, there are two kinds of transistors available: LV (low-voltage) and HV (high-voltage). LV device is designed for digital function, with the supply voltage below 1.2V. HV device is added for supply voltage up to 3.3V, which is a popular I/O standard. The HV device can achieve higher DC gain due to smaller channel length modulation. For the modified CMOS inverter, both input transistors M_{n1} and M_{p1} are built with HV devices, while the cascode transistors M_{n2} and M_{p2} are built with LV ones. This combination achieves DC gain of 60 dB easily. To disable a certain unit of CMOS inverter, gates of cascode devices are tied to the power rail, by opening S_2 and

closing S_1. This switching configure reduces the capacitive load to the current-mode comparator. For CMOS inverter, the minimum supply voltage is the threshold voltage sum of NMOS and PMOS transistors. So the supply voltage is set to 1 V.

The simulation result of GBW and phase margin is shown in Figure 5.18.

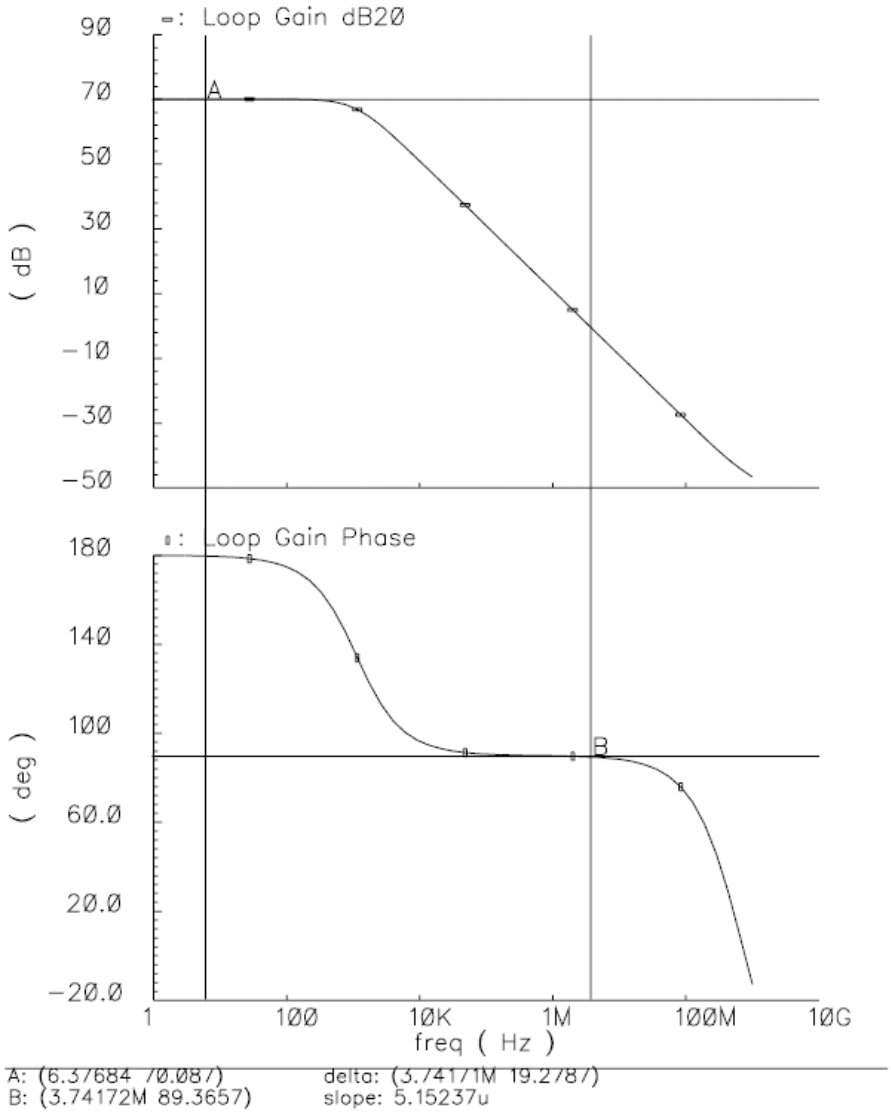

Figure 5.18: Simulation result for OTA (N=2).

5.3.3 Current-mode Comparator

The comparator plays a critical role for the performance of SAR ADC. A current-mode latched comparator is adopted in this design. The detailed schematic is shown in Figure 5.19. It is built with a cross-couple latch (M_{p1}, M_{p2} and M_{n1}, M_{n2}), and two

diode-connected inverters (M_{n3} and M_{p3}, M_{n4} and M_{p4}). The driving strength of each diode is set as twice of that from the latch. The operation of comparator contains two phases: sensing and regeneration. During sensing period, S_1, S_2 and S_3 are all closed. The input current is converted into a voltage by the diode-connected inverters, which sets the initial voltage for latch regeneration. The latch starts regeneration right after S_1 and S_2 are opened. The opening of S_3 is delayed by a short time. This attenuates the switch error from S_3 by the regeneration factor, which is similar to [59]. To compare the current difference between PMOS and NMOS (in Figure 5.3) with zero, V_{ip} is connected to OTA output and V_{in} is floating. Both S_1 and S_2 are close to power rail, single PMOS and NMOS transistors with minimum size are used, in order to reduce switch error.

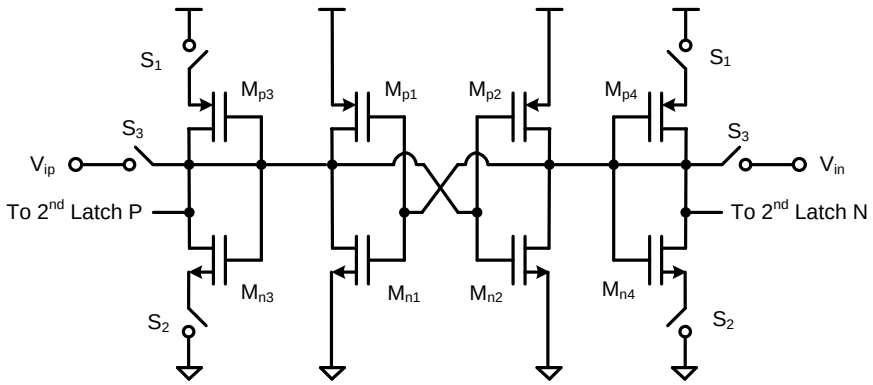

Figure 5.19: The detailed schematic for current-mode latched comparator.

Because both OTA and comparator diodes are implemented with CMOS inverters, there is a "short-circuit" path during sensing period. This extra current path increases the power consumption, especially when ADC input is close to power rail (VDD), shown in Figure 5.20. From circuit simulation, only 10% additional power is required for inputs close to power rail, compared with inputs around $V_{DD}/2$. This is mainly due to faster conversion rate. This issue is solved by the programmability of S_3 in Figure 5.20 (S_3 in Figure 5.3 also), which is comprised of a NMOS transistor and a PMOS

transistor. These two transistors can be enabled independently. When the ADC input is close to ground, the V_g is high and the OTA output is close to ground, during first few SAR cycles. To cut the "short-circuit" path, only PMOS transistor in S_3 is enabled. Vice verse, only NMOS transistor is enabled when ADC input is close to V_{DD}. For the targeted sensing system, this manually adaptive scheme is feasible, because the ADC input range is fairly predictable. The simulated power saving from "disable PMOS" and "disable NMOS" is shown in Figure 5.21.

A better solution is shown Figure 5.22, which was figured out after fabrication. The idea is to prevent V_g from approaching power rail, using feedback.

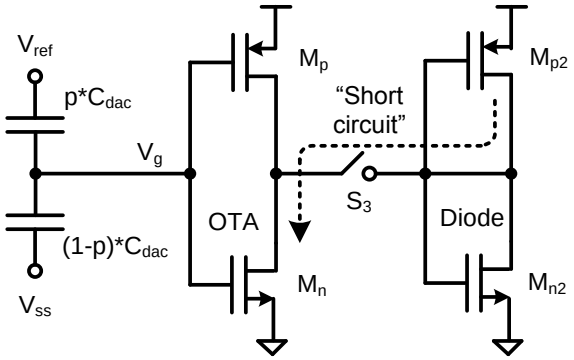

Figure 5.20: "Short circuit" path during SAR approximation.

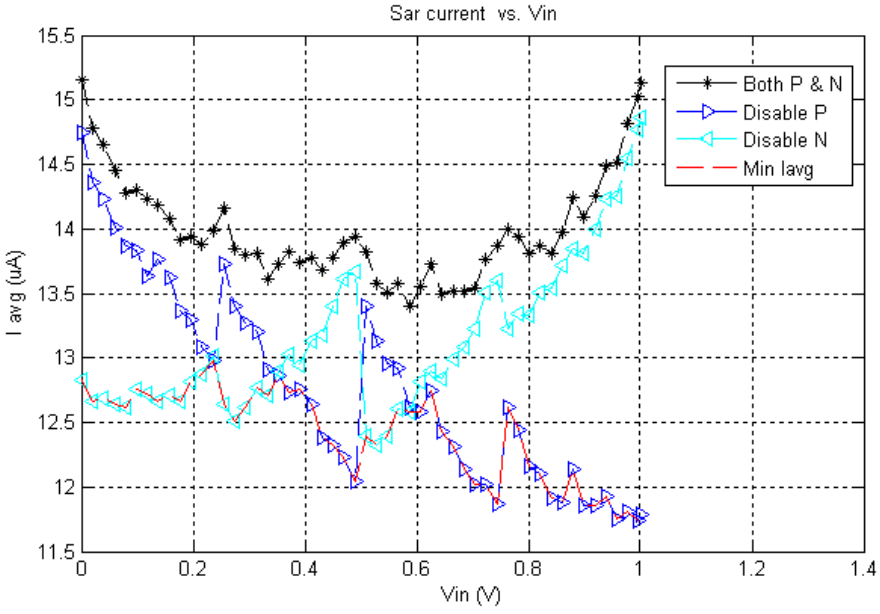

Figure 5.21: Power saving using adaptive switching.

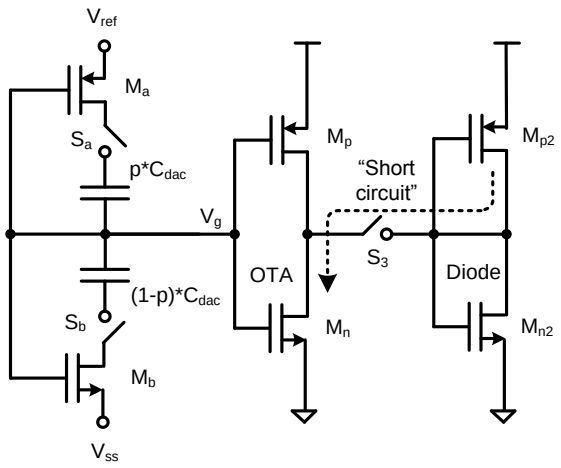

Figure 5.22: Better solution for "short circuit" path.

The latch outputs after regeneration is sensed by the second latch, which is implemented in Figure 5.23. During sensing period of comparator, the 2nd latch is in preset state, in which S_1 is close and S_2 is open. Node X is forced to supply voltage and D_{out} is set as logic high. During regeneration period, S_1 is open and S_2 is close. If V_c exceeds the inverter threshold, node X is discharged and D_{out} is set as logic low. After "comparison done", S_2 is open to save power, and the cross-coupled latch is enabled to keep the comparison result for SAR engine. Please note the cross-coupled latch is in open loop during the preset period. Because D_{out} is preset as logic high, one simple *NAND2* gate is used to generate "comparison done" signal, from the output of "2nd latch P" and "2nd latch N" (in Figure 5.19).

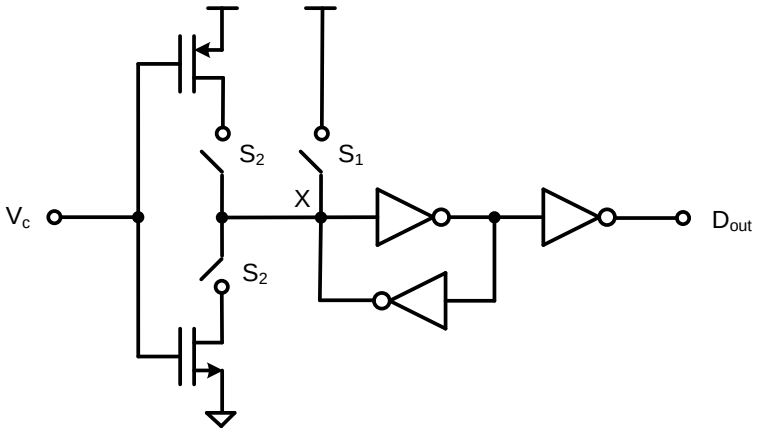

Figure 5.23: The schematic for 2nd latch.

5.3.4 SAR Engine and Phase Generator

For SAR ADC, the proper operation is controlled by SAR engine and phase generator. For phase generation, non-overlapping clock scheme is applied conventionally. To prevent overlapping, design margin is required for the non-overlapping period. This delay reduces effective settling time, while consuming more current. For this implementation, the inherent delay for control signal is utilized. For example, in Figure 5.3, S_1 should be opened before S_2, in order to avoid signal dependent switch error. To satisfy this timing requirement, the generated control signal is firstly routed to S_1 during layout, and then routed to S_2 with minimum buffer. This routing scheme guarantees that S_2 is always opened after S_1. The same method is used for the whole design.

The SAR engine contains two portions: shifting register and data register. The shifting register defines try-and-clear sequence from MSB to LSB, while data register stores the comparison result for each bit. To save power, both shifting register and data register are implemented in latch-based style, instead of DFF-based one. The latch-based design reduces logic fan-out for the clock tree, which has highest toggling rate in SAR ADC. Meanwhile, smaller area is achieved with latch-based design. The latch for data registers is shown in Figure 5.24, with clock contained in "Init_0/1".

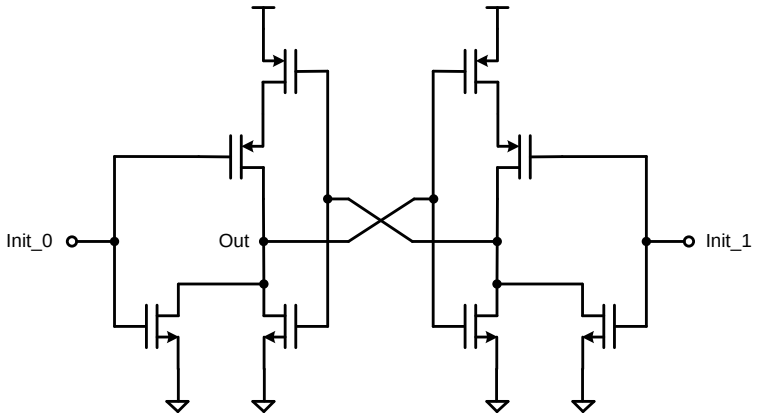

Figure 5.24: The latch used in data registers.

5.3.5 Switches

Switches play an important role in switched-capacitor circuits. The feedback switch (S_0 in Figure 5.3) is implemented as shown in Figure 5.25. To reduce the ON resistance, the N-well for the PMOS transistors M_{p1} is shorted to OTA output when the switch is closed, which reduces its bulk effect; it is connected to *VDD* when the switch is opened.

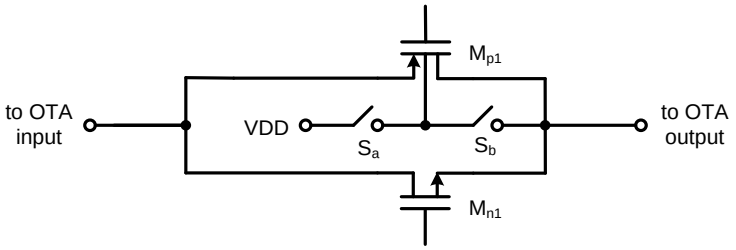

Figure 5.25: The schematic for the feedback switch.

The switch array for the capacitor array is shown in Figure 5.26. For the PMOS M_{p1}, same configuration as Figure 5.25 is used to reduce its ON resistance.

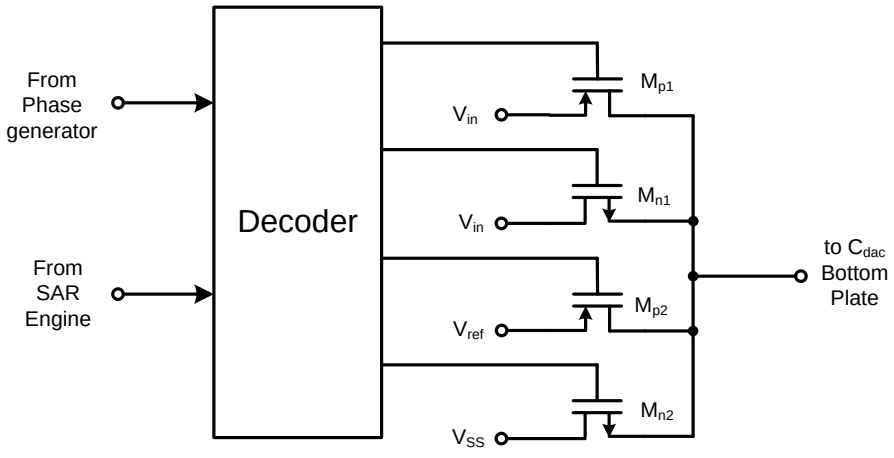

Figure 5.26: The switch for capacitor array.

5.3.6 Offset Cancellation for the Sampling Switch

For the proposed SAR ADC, the input sampling is completed by opening S_1 in Figure 5.3. This switch introduces switch error: charge injection and clock feedthrough.

However, because the voltage at S_1 is always at V_{cm1} when opening, the switch error is translated into offset error in the ADC results. This error can be reduced by adding dummy transistors. However, its effect depends on the transition rate of the clock [60]. For this SAR ADC, one offset cancellation technique, shown in Figure 5.27, is explored.

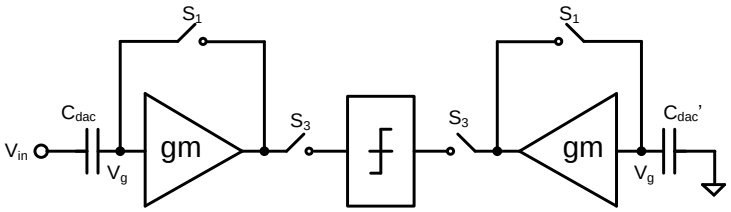

Figure 5.27: The offset cancellation for sampling switch.

The offset cancellation works in a pseudo-differential way, with duplicating the OTA and C_{dac}. Because the current-mode comparator already contains both positive and negative inputs, the integration with this SAR ADC is fairly straightforward. In order to implement this feature with small area, the additional C_{dac}' is implemented with MOS capacitor. Assuming the error voltage on C_{dac} and C_{dac}' is V_e and V_e', the input referred offset error can be calculated as V_e-V_e', which is smaller than the offset error (V_e) in Figure 5.3. Please note this feature is added to explore its possibility; it won't be included in the publication.

5.4 Experimental Results

The design is implemented in a 0.13 μm CMOS technology. The layout view is shown in Figure 5.28, while the die photo is shown in Figure 5.29. The design size for SAR ADC is 340 μm * 320 μm. The test chip is assembled in a QFN package. Both supply voltage and reference voltage are set as 1.0 V. A programmable DC source, Yokagawa 7651, is used to generate DC input signal. No external biasing is required. The PCB used for evaluation is show in Figure 5.30.

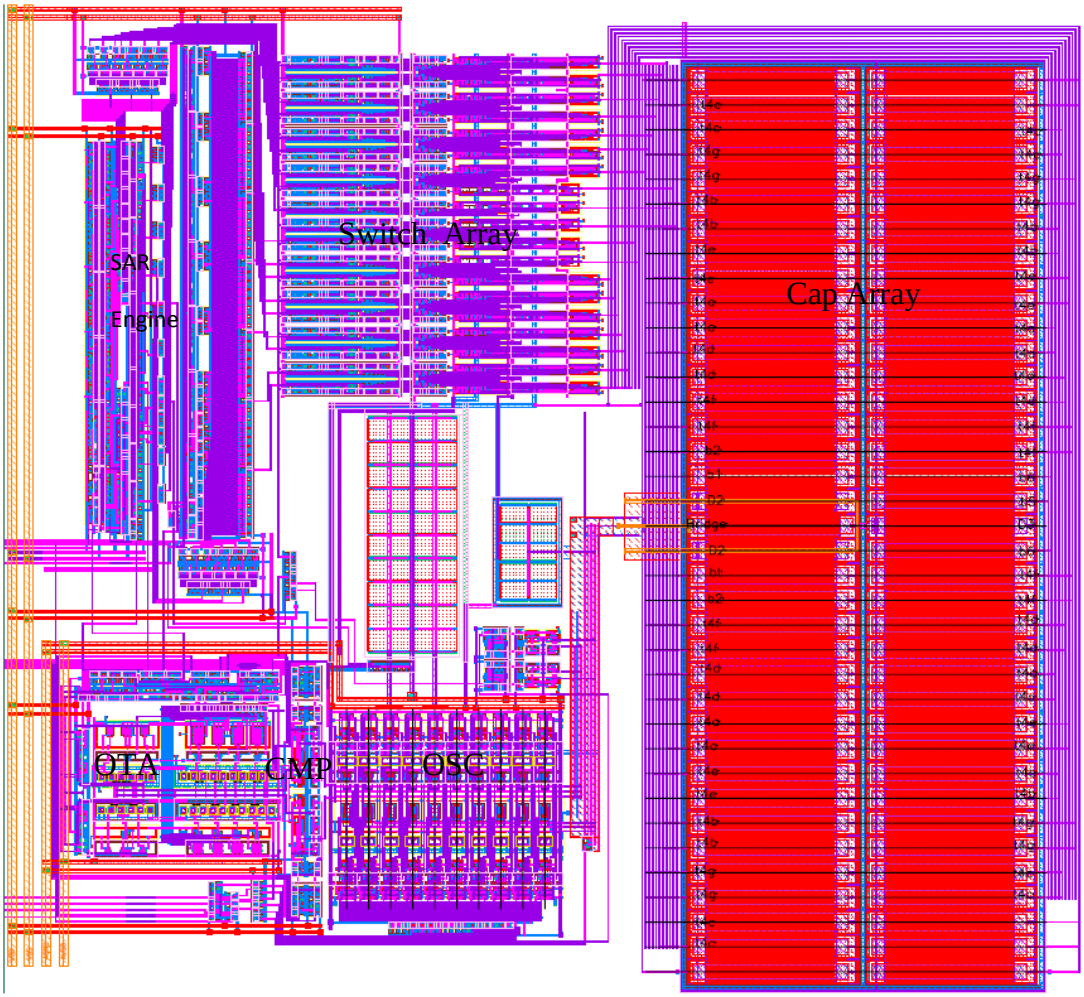

Figure 5.28: The layout view.

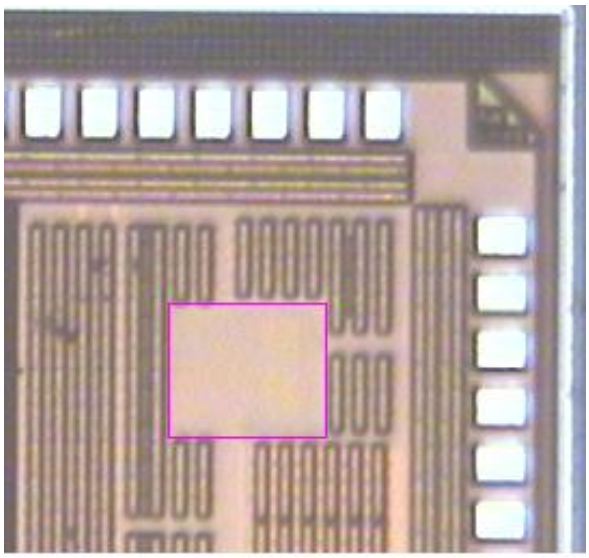

Figure 5.29: The die photo.

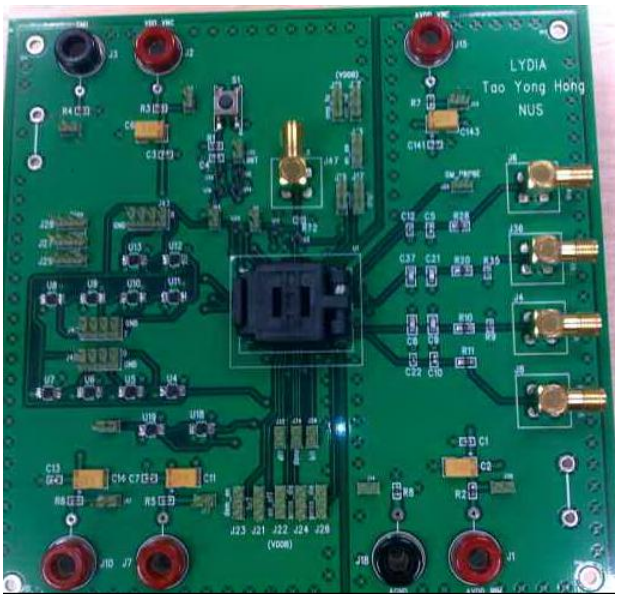

Figure 5.30: The PCB for DUT evaluation.

The measured differential nonlinearity (DNL) error and integral non-linearity (INL) error are shown in Figure 5.31. The maximum DNL is -0.31/+0.37 LSB, while the maximum INL is -0.30/+0.36 LSB. Careful layout is the main reason for such small errors. Please note the DEM is disabled during measurement, because of small mismatching error. The INL and DNL with DEM enabled are shown in Figure 5.32.

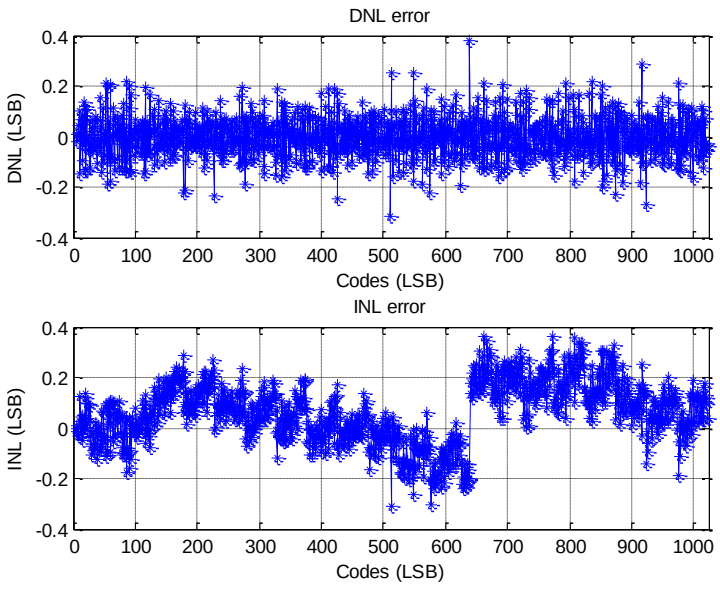

Figure 5.31: The measured INL and DNL error with DEM disabled.

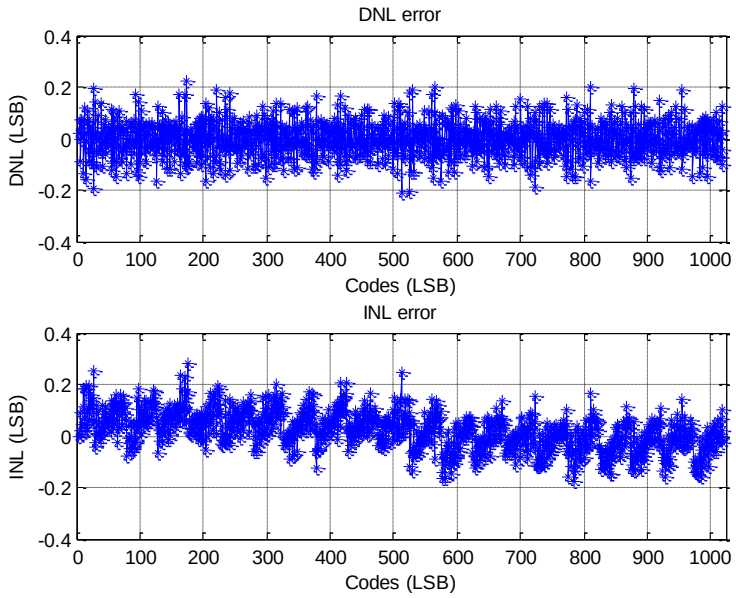

Figure 5.32: The measured INL and DNL error with DEM enabled.

The measured offset error is about 2 LSB. The small offset error is achieved by using current-mode comparator, with V_{cm} buffer as the pre-amplifier. The offset due to the switch error from S_1 (in Figure 5.3) is attenuated by large C_{dac} of 2.56 pF. Please note, the offset cancellation is disabled during measurement, because its effect is small. This is mainly because S_1 in Figure 5.25 is built with a NMOS transistor and a PMOS transistor, with same size. The switch error is almost cancelled between them.

Although this ADC is only for slowly varying or sampled DC signals, a sine wave of 49.99 kHz frequency is applied, for the purpose of performance comparison. The FFT spectrum with 131072 points is shown in Figure 5.33. The measured peak SNDR is 56 dB and the peak SNR is 58 dB.

With clock frequency of 16 MHz and conversion rate of 1 MS/s, the power consumption (excluding that from reference supply) is 18 μW under supply voltage of 1.0 V, in which the analog portion consumes 10 μW, and the digital portion consumes 8 μW. With the calculated effective number-of-bits (ENOB) of 9, the figure-of-merit (FOM) is 35 fJ/conversion. Please notes *FOM* is defined as (not based on ERBW)

$$FOM = \frac{P}{Fs * 2^{ENOB}}, \qquad (5.7)$$

instead of $FOM = \frac{P}{2 * ERBW * 2^{ENOB}}$, where, P is the power consumption, Fs is the conversion rate, ERBW is effective resolution bandwidth. This is because the targeted application is to convert the DC inputs from multiple input channels. The low power consumption is achieved with reusing the OTA as the pre-amplifier of current-mode comparator. Meanwhile, the whole ADC works without any additional reference generator and biasing circuit, by using a modified CMOS inverter as the amplifier. Low power digital circuits also contribute. The power consumption for each portion is shown in Figure 5.34. Please note the power consumption for each block is from post-layout simulation instead of silicon evaluation, because of shared power bus.

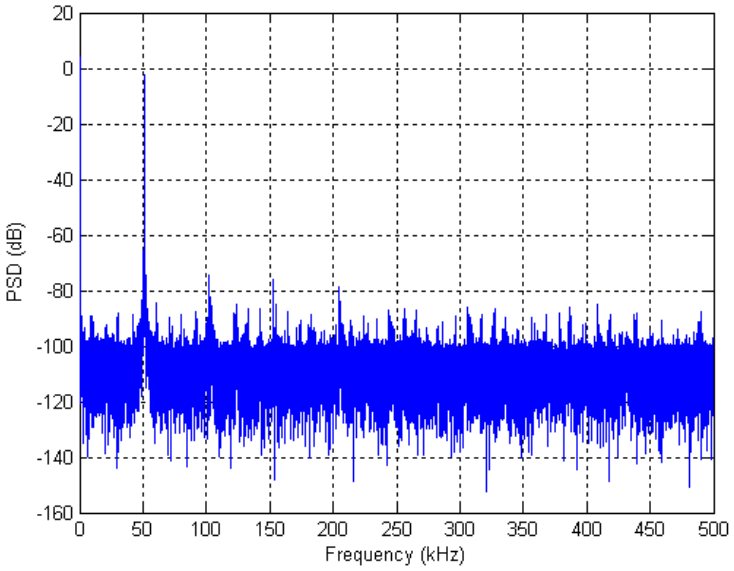

Figure 5.33: The measured FFT spectrum with sine input of 49.99 kHz.

The power consumption from the reference voltage is checked. However, the improvement from dual thermometer decoders is almost invisible. The main reason is to use polysilicon as shielding layer of capacitor array, which increased the parasitic capacitance (to ground) of bottom plate significantly. The experimental result is

summarized in Table 5.5. The comparison with others' work (in single-ended only) is shown in Table 5.6. Note that the offset error from [29] and [28] should be much larger than this work, because of lack of pre-amplifier.

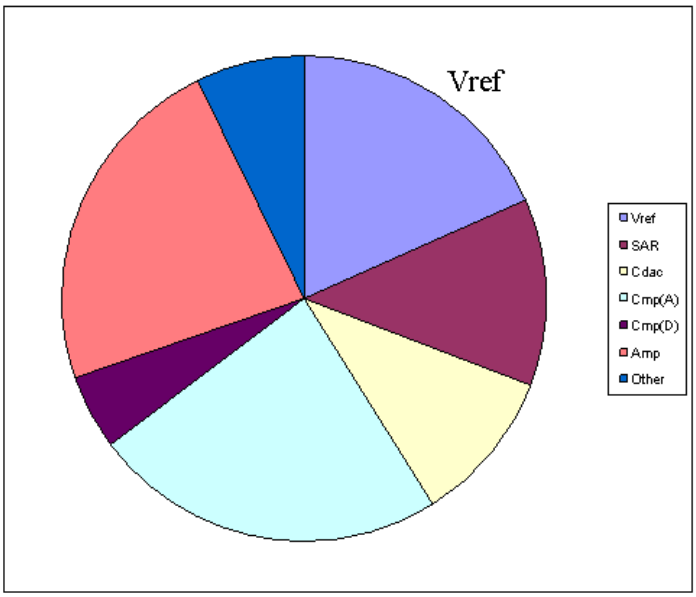

Figure 5.34: The power consumption for each block (in clockwise order).

Table 5.5: The summary for experimental results.

Items	**Results**
Supply voltage	1.0 V
Reference voltage	1.0 V
Conversion rate	1 MS/s
Maximum DNL	-0.31/+0.37 LSB
Maximum INL	-0.30/+0.36 LSB
Offset error	2.00 LSB
Peak SNR/SNDR	58/56 dB
ENOB	9 bit
Power consumption	18 μW
FOM (based on F_s)	35 fJ/conversion

Table 5.6: Performance comparison.

Items	**This work**	[29]**, 2008**	[28]**, 2007**
Supply voltage (V)	1.0	1.0	0.9
Process (μm)	0.13	0.18	0.18
Conversion rate (kS/s)	1000	100	200
Resolution (bit)	10	12	8
Need external biasing?	No	Yes	No
DNL (LSB)	-0.31/+0.37	-2.00/+1.60	-0.90/+0.26
INL (LSB)	-0.30/+0.36	-2.50/+2.50	-0.53/+0.50
ENOB (bit)	9.0	9.4	7.58
Power (μW)	18	3.8	2.47
FOM (fJ/conv) $FOM = \frac{P}{Fs * 2^{ENOB}}$	35	56	65
FOM (fJ/conv) $FOM = \frac{P}{2 * ERBW * 2^{ENOB}}$	---	56	65

5.5 Conclusions

A low voltage, low power, single-ended SAR ADC for sensing system has been presented. To reduce power consumption, the OTA for common-mode buffer is reused as the pre-amplifier for current-mode latched comparator. The OTA is built with a modified CMOS inverter, assisted with an adaptive technique to account for process, supply and temperature variations. Overall, this ADC does not require additional reference generator and biasing circuits. Meanwhile, a split capacitor array with dual thermometer decoders is proposed, in order to reducing switching energy.

CHAPTER 6 A 0.8-V, 1-MS/S, SAR ADC FOR SENSING SYSTEMS

6.1 Introduction

For the sensing systems, the power efficiency is critical due to the nature of the application. In this work, we present several techniques to further improve the power efficiency of the single-ended SAR ADC, based on the results in previous chapter. Firstly, a small capacitor is put in series with the C_{dac} such that the load of V_{cm} buffer during input tracking is significantly reduced. This lowers the amplifier's power consumption. Secondly, the V_{cm} buffer is reused as the pre-amplifier of a current-mode comparator. The input referred offset error from the latched comparator is reduced. Lastly, dual thermometer decoders are introduced to the split capacitor array to reduce both switching energy and DNL error at the same time.

This paper is organized as follows. After the introduction, we present the ADC architecture and timing allocation in Section II. The implementation of various building blocks is discussed in Section III. Section IV presents the experimental results and Section V concludes this work.

6.2 Architecture Design

The proposed single-ended SAR ADC is illustrated in Figure 6.1, which comprises of a capacitor array, i.e. C_{dac}, two small capacitors C_a and C_b, a shared OTA, a current-mode latched comparator, a SAR engine and a switch array (S_4 and S_5). It supports

rail-to-rail input range, with supply voltage as the reference level. The switch S_b is an assumed one, which is implemented inside the OTA in a switched-opamp style.

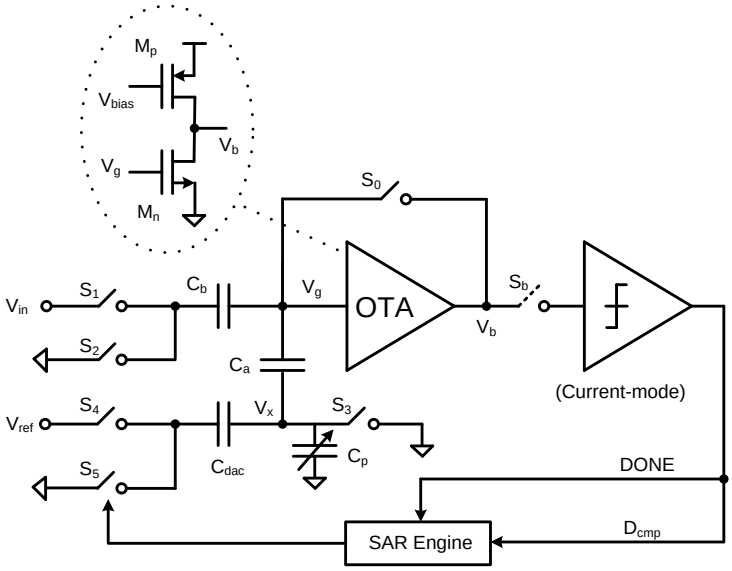

Figure 6.1: The Proposed SAR ADC.

The OTA is built with a simple common-source amplifier, which eliminates the generation of a real V_{cm} voltage, by auto-zeroing between input tracking phase and successive approximation phase. During input tracking, the switches S_0, S_1, S_3 and S_5 are closed while S_2 and S_4 are opened. With negative feedback, V_g is forced to a common mode voltage, referred as V_{cm1}, which is defined by the relative driving strength between M_n and M_p. V_{cm1} can be set around $V_{DD}/2$ easily with the V_{DD} of 0.8 V. After settled, the charge stored at V_g node is

$$Q_{sample} = (V_{cm1} - V_{in}) * C_b + V_{cm1} * C_a , \qquad (6.1)$$

while the charge at V_x is

$$Q_{sample\_Vx} = (0 - V_{cm1}) * C_a \ . \qquad (6.2)$$

The current flowing through M_n and M_p should be equal, by assuming an opened S_b. The input sampling is completed by the opening of S_0, followed by the opening of S_1 and S_3 and closing of S_2. This clocking scheme eliminates signal-dependent charge

injection and clock feedthrough from S_1. The switch error from S_0 results in offset error due to small C_a and C_b. This is compensated by the digital calibration, which is illustrated in section III.

During successive approximation period, the assumed switch S_b is closed. To decide the MSB, half of C_{dac} is connected to V_{ref} through S_4 while another half to ground. The current-mode comparator performs a comparison between the current flowing through M_p and M_n. If the current through M_p is larger than that through M_n, the comparator result is set as high. The SAR engine and switching array adjusts the voltage divider inside C_{dac} to raise V_g through C_a, which increases the current through M_n. After ten cycles of successive approximation, the current through M_p is almost equal to that through M_n, with quantization error and offset as the residue. Depending on the implementation of current-mode comparator, the voltage at the OTA output after SAR convergence may be different from V_{cm1}, which is its potential during input tracking. This makes V_g deviate slightly from V_{cm1}. The V_g after SAR convergence is referred as V_{cm2}, and the charge at V_g node is

$$Q_{conv} = (V_{cm2} - V_{xc}) * C_a + V_{cm2} * C_b ; \qquad (6.3)$$

while the charge at V_x node is

$$Q_{conv\_Vx} = (V_{xc} - V_{cm2}) * C_a + V_{xc} * C_p + p * C_{dac} * (V_{xc} - V_{ref}) + (1-p) * C_{dac} * V_{xc} , \qquad (6.4)$$

where V_{xc} is voltage of V_x after SAR convergence. With the law of charge conservation at both V_g and V_x nodes, V_{in} can be calculated as

$$\begin{aligned} V_{in} &= p * V_{ref} * \frac{C_a}{C_b} * \frac{C_{dac}}{C_a + C_p + C_{dac}} + m * (V_{cm1} - V_{cm2}) \\ V_{in} &= p * V_{ref} * \frac{C_a}{C_b} * \frac{C_{dac}}{C_a + C_p + C_{dac}} + m * (V_{oc} - V_{cm1}) / A \end{aligned} , \qquad (6.5)$$

where, V_{oc} is the OTA output after SAR convergence and A is the DC gain of OTA, m is

$$m = 1 + \frac{C_a}{C_b} - \frac{C_a}{C_b} * \frac{C_a}{C_a + C_p + C_{dac}} \ . \qquad (6.6)$$

To eliminate the gain error (with C_a larger than C_b), we have to set

$$\frac{C_a}{C_b} * \frac{C_{dac}}{C_a + C_{dac} + C_p} = 1 \ . \qquad (6.7)$$

This can be achieved by making C_p tunable. The value of C_b is determined by the kT/C noise requirement. With process variation such as capacitor mismatch taken into consideration, the C_a is set slightly larger than its calculated value in order to facilitate the gain error compensation through the tunable C_p. With C_{dac} connected to the amplifier through C_a, the amplifier's capacitive load during input tracking is reduced from C_{dac} in chapter 5 to C_a+C_b. This in turn lowers the power consumption of the common-source amplifier. The load to its analog front-end is also reduced to C_b, which lowers the power consumption of the whole sensing systems. In this design, both C_a and C_b are close to 250 fF, while the equivalent capacitance of C_{dac} is around 2.56 pF. The penalty of putting C_{dac} in series with C_a is to increase the sensitivity requirement from the comparator by a factor of (C_a+C_b)/C_a. This drawback is relaxed by allocating a shorter period for input tracking with less capacitive load to the OTA, compared with that using C_{dac} as the load. This leaves more time for the comparator. In addition, in section III some techniques are introduced to reduce the capacitive load to the current-mode comparator. This speeds up the comparator in order to achieve higher sensitivity.

To make sure the PN junctions inside all the switches are not forwardly biased during successive approximation, multiple spectre simulations are executed. For this SAR ADC, the two critical nodes are V_x and V_g, whose waveform during SAR converging are shown in Figure 6.2 and Figure 6.3 respectively.

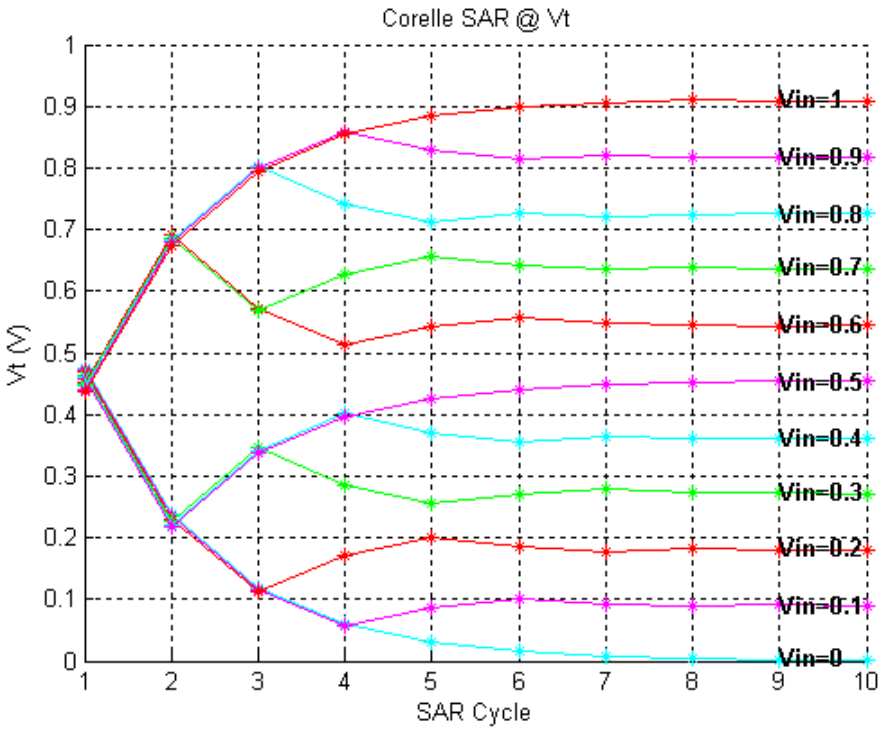

Figure 6.2: The SAR converging of V_x node with different V_{in}.

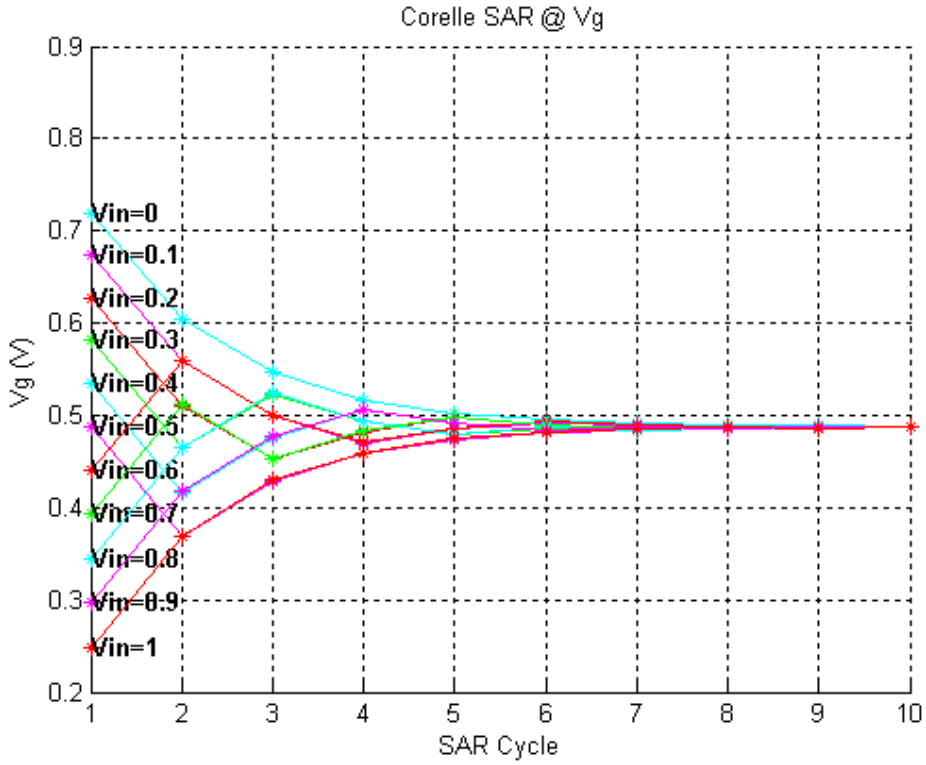

Figure 6.3: The SAR converging of V_g node with different V_{in}.

After gain error been corrected, m can be simplified to C_a/C_b. With high enough DC gain (about 60 dB), the error due to the discrepancy between V_{cm1} and V_{cm2} is ignorable. In addition, the comparator offset error in current-mode is attenuated by the OTA's transconductance before referring back to V_{in}. In this sense, the OTA is reused as the pre-amplifier of the current-mode comparator. There are several advantages in the use of current-mode comparator, compared with voltage-mode one. Firstly, it eliminates the generation of common mode voltage, because the comparison is performed between zero and the current difference through M_p and M_n. Secondly, it has low input impedance, which turns the OTA output into a low impedance node. This speeds up the conversion and reduces the power consumption indirectly. Lastly, the initial voltage of latch regeneration can be set around $V_{DD}/2$. This reduces comparator dynamic offset due to capacitance mismatch, compared with the dynamic latch [56]. One drawback of current-mode comparator is the static current consumption. However, its benefits justify this additional cost.

The comparator also generates a "comparison done" signal, which is used by the SAR engine to initiate C_{dac} settling for next bit cycle, right after the comparison decision is made. This increases the settling time for C_{dac} and current-mode comparator. The power consumption is reduced indirectly. The timing diagram is shown in Figure 6.4. The SAR conversion is completed in 12 clock cycles, in which 2 cycles for input tracking and 1 cycle for each SAR bit. The allocated number of cycles for input tracking is determined by the trade-off of power consumption among OTA, current mode comparator and digital circuits. Another consideration is OTA's transconductance, which attenuates the comparator's offset in current-mode, before referring back to ADC input. During the high period of *CLK*, the current-mode comparator senses the current difference between M_p and M_n. At the falling edge of

CLK, the comparator is strobed and starts regeneration. At the rising edge of *DONE* signal, *Sar*[5] is set to high while *Sar*[6] is cleared. The C_{dac} settling for bit[5] starts immediately. For SAR ADC, critical decision (SAR result close to final value) does not span two consecutive cycles. This property increases C_{dac} settling time for the critical decision, which improves converter accuracy and reduces total power consumption indirectly.

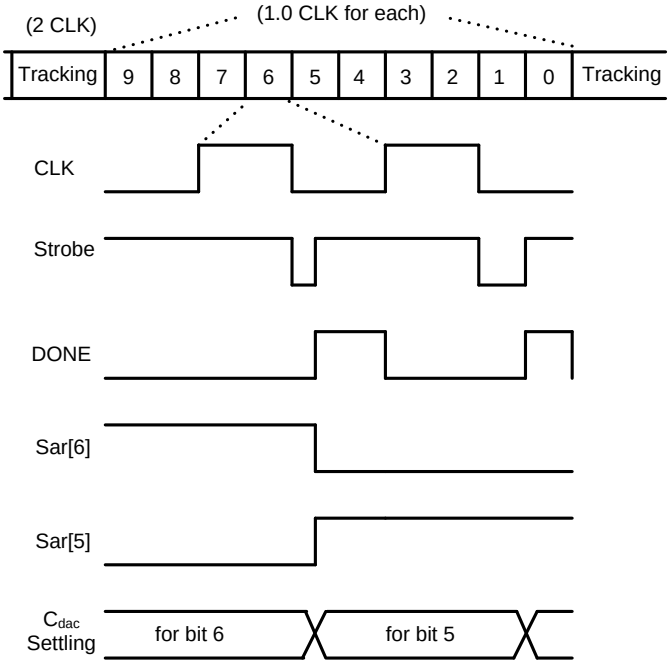

Figure 6.4: The timing diagram.

6.3 The Implementation of SAR ADC

6.3.1 Operational Transconductance Amplifier (OTA)

The operational transconductance amplifier (OTA) is the most critical design block for this SAR ADC. Its transconductance g_m decides the time constant (*TC*) of the settling during input tracking by

$$TC = (C_a + C_b) / g_m . \qquad (6.8)$$

For high-speed SAR ADC, the input tracking is completed in a short time. The OTA's power efficiency directly determines the figure-of-merit (FOM) of whole ADC. To drive a large capacitive load, a single-stage OTA has highest power efficiency, in which the loaded capacitor is used for compensation implicitly. However, single-stage OTA is not suitable for tracking of high frequency signals, because the OTA gain starts dropping far below the Nyquist frequency. The low amplifier gain at high frequency is not able to maintain a stable common mode voltage under fast-varying inputs. This is not an issue for the targeted sensing systems, with slowly varying or sampled DC signals as inputs.

Figure 6.5 lists three topologies of single-stage OTA. For comparison, the power efficiency is defined as

$$E = g_m / I \,, \qquad (6.9)$$

where I is total current consumption. The power efficiency of common-source amplifier in Figure 6.5B is normalized as 1. For the differential pair in Figure 6.5A, two current branches are included. However, only one of them contributes the effective transconductance; so the power efficiency is halved. For the CMOS inverter in Figure 6.5C, there is only one current branch, which is used by both PMOS and NMOS to double the transconductance and power efficiency. Meanwhile, the CMOS inverter has best slew behavior. Dependent on input polarity, this amplifier can sink or source large current in short time. However, for common-source amplifier, the positive slew is limited by the PMOS active load. In the differential pair, both positive and negative slew rate are limited by the same tail current.

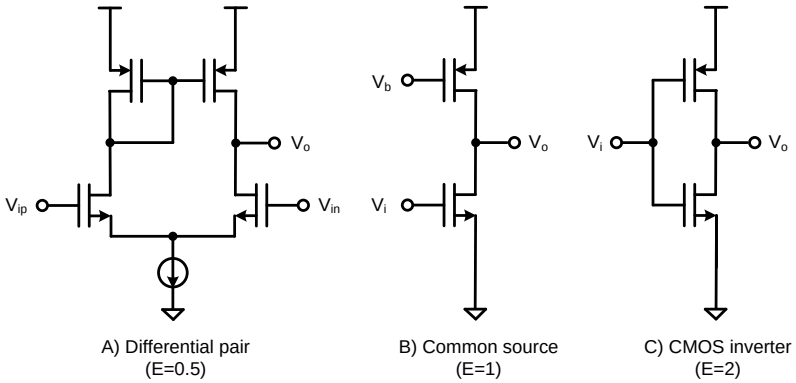

Figure 6.5: Three topologies for single-stage OTA.

During input tracking, large transconductance and slew rate shorten the settling time. For the highest power efficiency, CMOS inverter should be the best out of the three topologies. However, its minimum supply voltage is $V_{thn}+V_{thp}$ (plus some headroom), where V_{thn} and V_{thp} are the threshold voltage for NMOS and PMOS transistors respectively. On the contrary, the minimum supply voltage of common-source amplifier is only V_{thn}. In order to operate this SAR ADC at 0.8 V, the common-source amplifier is selected.

The detailed schematic of the common-source amplifier is shown in Figure 6.6. During input tracking, both M_{p2} and M_{n2} are on while M_{p3} and M_{n3} are off, by setting V_s to V_{DD}. Both M_{p2} and M_{n2} are in saturation region with V_{DD} of 0.8 V and work as cascode devices for the common source amplifier composed of M_{n1} and M_{p1}. In this design, the current reference V_{bias} is provided from off-chip. It also can be implemented on-chip using a constant-g_m topology. During successive approximation period V_s is set to 0 and M_{p3} and M_{n3} work as cascode devices. As above, the assumed switch S_b in Figure 6.1 is implemented by two separate cascode paths. With this arrangement, the capacitive load to the comparator from the OTA side is the junction and overlap capacitance from M_{p3} and M_{n3}, which speeds up the comparator; otherwise the large parasitic from S_0 (in Figure 6.1) will slow down the comparator.

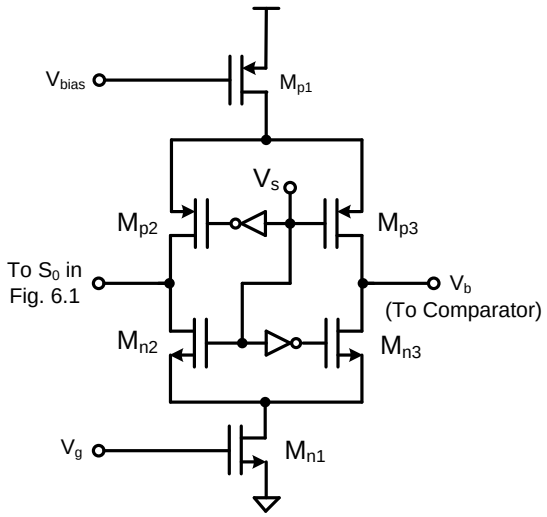

Figure 6.6: The detailed schematic for the amplifier.

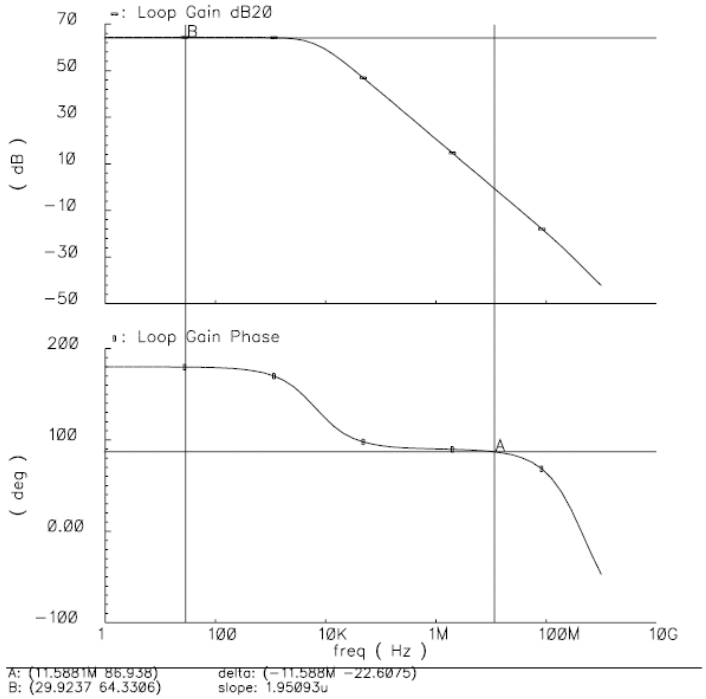

Figure 6.7: The simulated DC gain from OTA.

As mentioned in Section II, DC gain of 60 dB is enough to maintain a stable common mode and to get rid of the offset error due to the difference between V_{cm1} and V_{cm2}. For the CMOS technology used, there are two kinds of transistors available: LV (low-voltage, thin gate oxide) and HV (high-voltage, thick gate oxide). LV device is designed for digital function. HV device is added for supply voltage up to 3.3V,

which is a popular I/O standard. The HV device can achieve higher DC gain due to smaller channel length modulation. To achieve the DC gain of 60 dB, HV devices are used for all those transistors M_{n1}~M_{n3} and M_{p1}~M_{p3}. The benefit of using HV devices for the cascode ones is to keep them in saturation region even under process variations. The spectre simulation result for DC gain is shown in Figure 6.7.

6.3.2 Current-mode Comparator

The comparator plays a critical role for the performance of SAR ADC. A current-mode latched comparator is adopted in this design. The detailed schematic is shown in Figure 6.8.

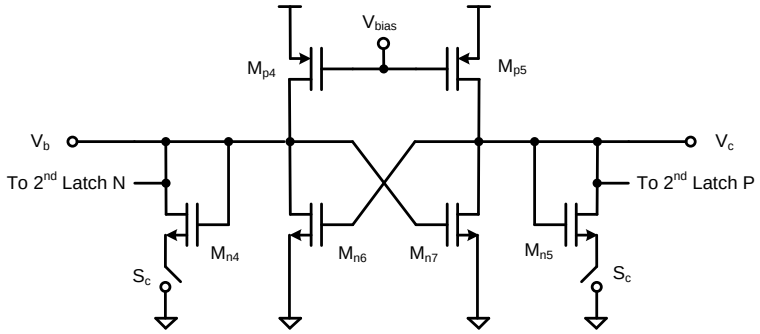

Figure 6.8: The schematic for the current-mode comparator.

The comparator is built with cross-couple M_{n6} and M_{n7}, and diode-connected M_{n4} and M_{n5}. The driving strength of M_{n4} and M_{n5} is twice of that from M_{n6} and M_{n7}. The operation of the comparator contains two phases: sensing and regeneration. During the sensing period, S_c is closed. The input current is converted into a voltage by the diode-connected M_{n4} and M_{n5}, which sets the initial voltage for latch regeneration. The latch starts regeneration right after the opening of S_c. To compare the current difference between M_n and M_p (in Figure 6.1) with zero, V_b is connected to the OTA output and V_c is floating. The switch S_c is close to power rail, a single NMOS transistor with minimum size is used, in order to reduce the switch error.

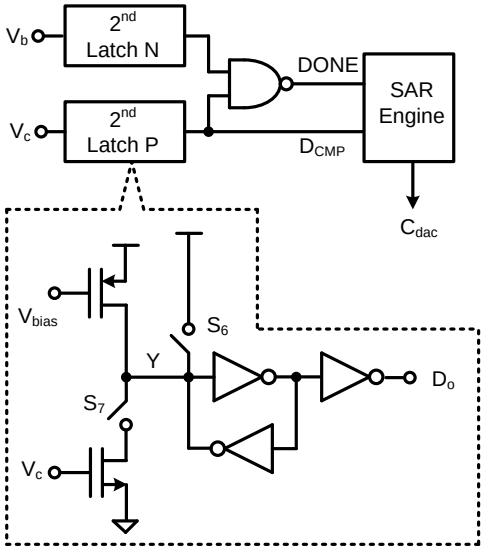

Figure 6.9: The schematic for 2nd latch.

The latch outputs after regeneration is sensed by the second latch, which is implemented in Figure 6.9. During the sensing period of the comparator, the 2nd latch is in preset state, in which S_6 is closed and S_7 is opened. Node Y is forced to supply voltage and D_o is set as logic high. During regeneration period, S_6 is opened and S_7 is closed. If V_c exceeds the inverting amplifier's threshold, node Y is discharged and D_o is set as logic low. After "comparison done", S_7 is open to save power, and the cross-coupled latch is enabled to keep the comparison result for the SAR engine. Please note the cross-coupled latch is in open loop during the preset period. Because D_o is preset as logic high, one simple NAND2 gate is used to generate the "comparison done" signal, from the output of "2nd latch P" and "2nd latch N".

6.3.3 The Capacitor Array

The linearity of SAR ADC is mainly decided by the accuracy of capacitor array, which is shown in Figure 6.10. To reduce the total number of capacitors, a split capacitor array [57] is adopted in this work. This topology has two drawbacks. Firstly, to get same accuracy, the size of unit capacitor, C_1 in Figure 6.10, is larger

than that in binary capacitor array. However, the total area is still smaller, because of much less capacitors included. Secondly, the parasitic capacitor C_{p2} in Figure 6.10, impacts the linearity of SAR ADC. This issue can be fixed by careful shielding and enlarging C_s.

Recently, the switching energy efficiency of capacitor array attracts a lot of attention [26]. In [58], the method of splitting MSB capacitor is proposed; however, its implementation is a bit complex. In this work, a simpler solution, with equivalent energy saving is proposed. As shown in Figure 6.10, two "3-to-7 thermometer decoders" are inserted into LSB and MSB portions respectively. Conventionally, thermometer decoder is used in capacitor array to reduce DNL error. However, its capability of reducing switching energy has not being explored. A 2-bit capacitor array is used here for easy illustration, as described in Table 6.1. Notes: C is the unit capacitor, V is the reference voltage.

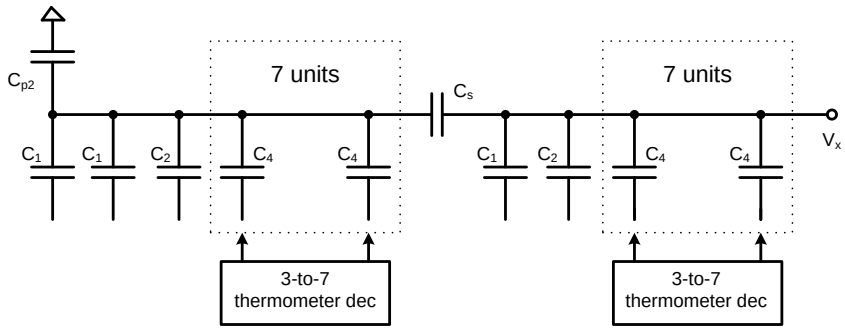

Figure 6.10: The capacitor array ($C_4 = 4C_1$, $C_2 = 2C_1$, $C_s = 32/31C_1$).

Table 6.1: The switching energy for 2-bit capacitor array.

Transitions	Binary	Thermometer
2→3	¼*CV2	¼*CV2
2→1	¾*CV2	¼*CV2

For a 2-bit SAR ADC, to decide the 2nd bit, there are two possible transitions: 2→1 and 2→3. For transition of 2→3, both thermometer and binary capacitor array consume the same switching energy ¼*CV^2. However, there is large difference for the transition of 2→1. For the binary weighted capacitor array, this transition contains two operations: discharging MSB capacitor to ground and charging LSB capacitor to reference voltage. It consumes less energy if these two operations are completed in two steps [58], compared with that from simultaneous jumps. Even with two-step operation, it consumes ¾*CV^2. For the thermometer weighted capacitor array, there is only a single operation for transition 2→1: discharging half of MSB capacitor to ground. It only takes ¼*CV^2 energy. For the detailed calculation of switching energy, please refer to [58]. Overall, the thermometer decoders reduce both DNL error and capacitor array switching energy.

The capacitor array is implemented with metal finger capacitor. To reduce parasitic capacitance C_{p2} in Figure 6.10, polysilicon and Metal 4 are used as shielding layers, which are connected to the bottom plate of C_{dac}. Only metal 1~3 are used for finger capacitors due to process limitation. With unit capacitor of 80 fF the equivalent capacitance of C_{dac} is about 2.56 pF.

6.3.4 Calibration Circuits for Gain and Offset Error

As mentioned in section II, the gain error is compensated by tunable C_p in Figure 6.1. The detailed implementation is shown in Figure 6.11, where C_{p1} is the inherent parasitic capacitor at V_x node. C_{g1}~C_{gn} is a binary weighted capacitor bank for gain error compensation. The offset error is corrected by another capacitor bank C_{o1}~C_{om}, whose bottom plate voltage is toggled between input tracking and successive approximation phase. For example, during input tracking, S_{o1} is closed and S_{o1b} is

opened. During successive approximation, S_{o1} is opened and S_{o1b} is closed, in order to inject negative charge to V_x node. To inject positive charge, vice verse.

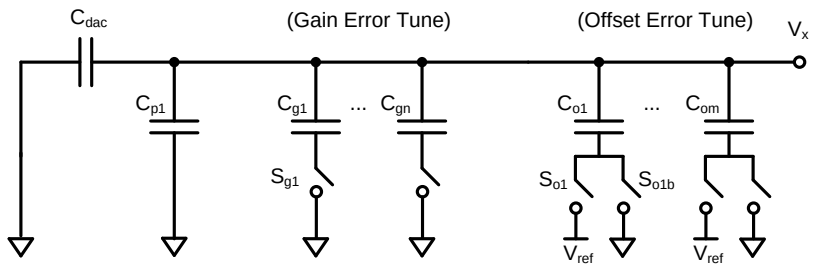

Figure 6.11: The tuning circuit for gain error and offset error.

For this SAR ADC, an 8-bit capacitor bank is used for gain error compensation, whose equivalent capacitance is plotted in Figure 6.12. The discontinuity is obvious in the plot due to some design redundancy. This is to ensure there is at least one digital code to map to any required capacitance even under process variation such as mismatching.

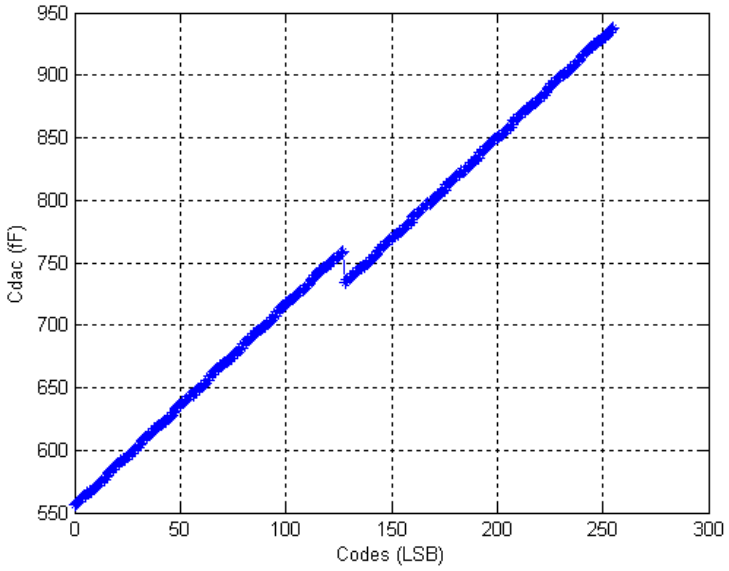

Figure 6.12: The capacitance for gain error compensation.

In addition, a behavioral simulation in MATLAB is utilized to check the effect of process variation. The results are shown in Figure 6.13.

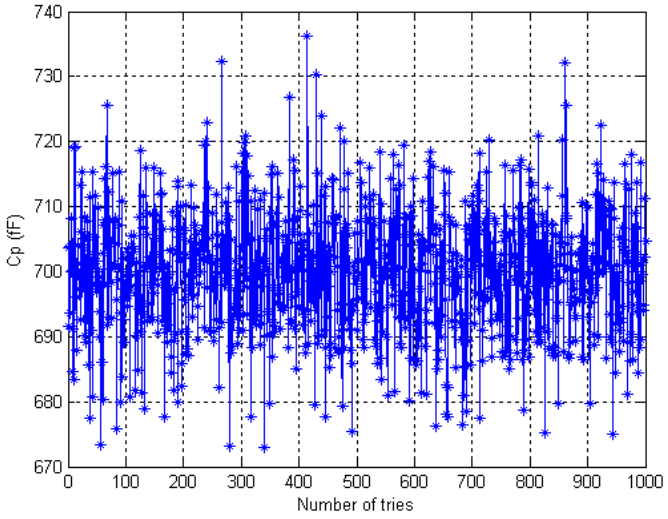

Figure 6.13: The variation of C_p due to process variations.

6.3.5 SAR Engine and Phase Generator

For SAR ADC, the proper operation is controlled by the SAR engine and phase generator. For phase generation, non-overlapping clock scheme is normally utilized. To prevent overlapping, design margin is required for the non-overlapping period. This delay reduces effective settling time, which consumes more current. For this implementation, the inherent delay of the control signals is utilized. For example, in Figure 6.1, S_0 should be opened before S_1, in order to avoid signal dependent switch error. To satisfy this timing requirement, the generated control signal is firstly routed to S_0 during layout, and then routed to S_1 with a buffer of minimum size. This routing scheme guarantees that S_1 is always opened after S_0. The same method is used for the whole design.

The SAR engine contains two portions: shifting register and data register. The shifting register defines try-and-clear sequence from MSB to LSB, while data register stores the comparison result for each bit. To save power, both shifting register and data register are implemented in latch-based style, instead of DFF-based one. The latch-based design reduces logic fan-out of the clock tree, which has highest toggling rate in

SAR ADC. Meanwhile, smaller area is achieved with latch-based design. The latch for data register is shown in Figure 6.14.

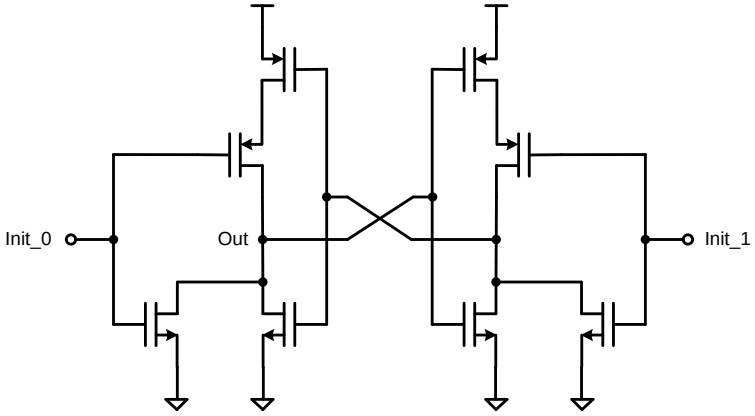

Figure 6.14: The latch for data register.

In addition, to demonstrate the concise layout for the SAR engine, its layout view is captured in Figure 6.15.

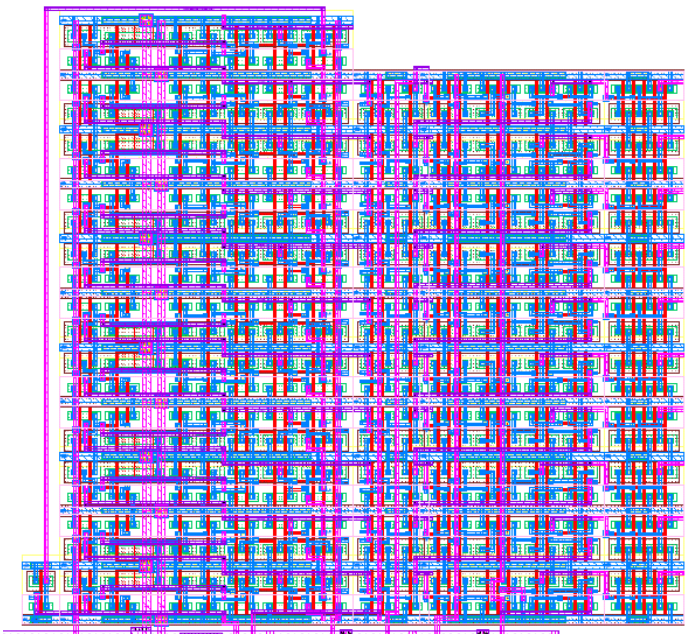

Figure 6.15: The layout view for the SAR engine.

6.4 Experimental Results

The ADC is fabricated in a 0.13 µm CMOS technology with an active area of 240 µm * 235 µm. The layout view is shown in Figure 6.16 while the die photo is shown in Figure 6.17. The V_{ref} and V_{bias} in Figure 6.6 are from off-chip. The pin-out is described in Figure 6.18. Both V_{DD} and V_{ref} are set to 0.8 V while the input is rail-to-rail. The test PCB is reused from the previous project in Chapter 5.

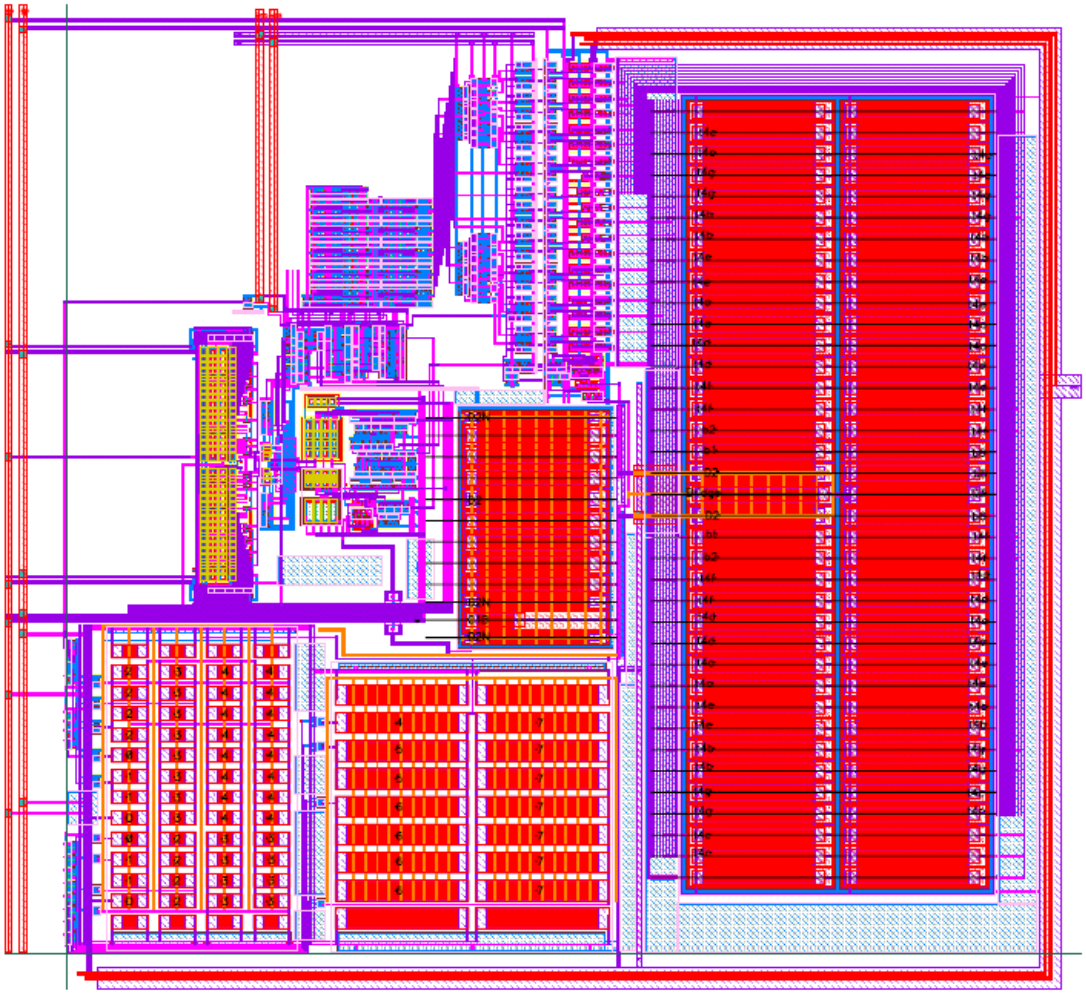

Figure 6.16: The layout view.

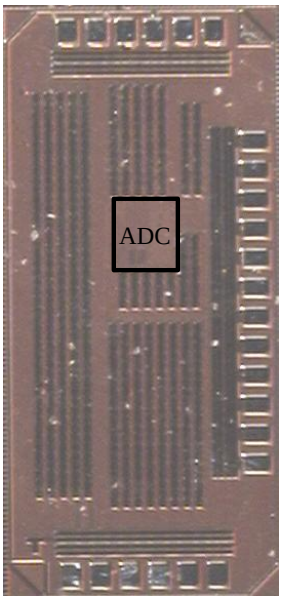

Figure 6.17: The die photo.

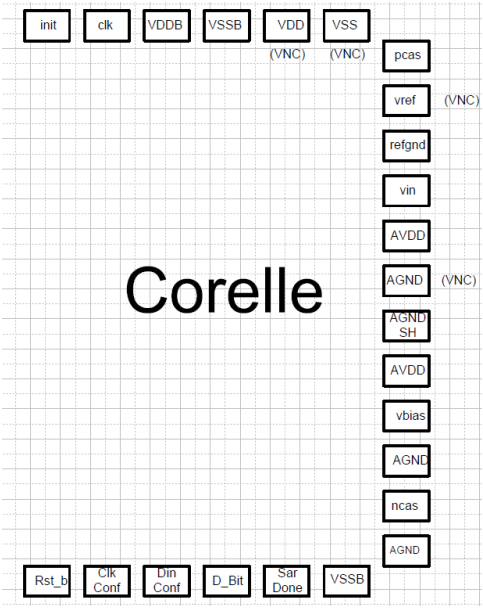

Figure 6.18: The pin-out for SAR ADC.

After gain error and offset error compensated, the measured the differential nonlinearity (DNL) error and integral non-linearity (INL) error are shown in Figure 6.19. The maximum DNL is -0.33/+0.56 LSB, while the maximum INL is -0.61/+0.55 LSB. The largest spike in DNL plot is consistent across all those measured chips, which indicates a systematic error and may be caused by foundry's metal filling.

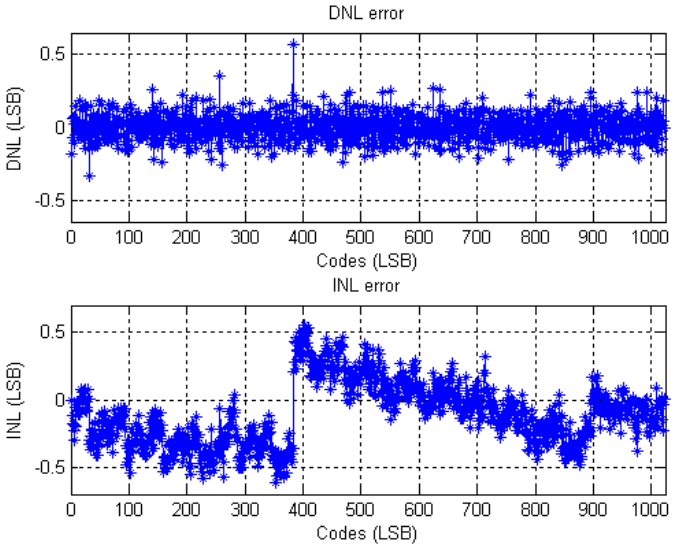

Figure 6.19: The measured DNL and INL errors.

Although this ADC is for slowly varying inputs, a sine wave with frequency of 49.99 kHz is applied for FOM comparison. The FFT spectrum is shown in Figure 6.21 with peak SNDR of 55 dB and peak SNR of 56 dB. With clock frequency of 12 MHz and conversion rate of 1 MS/s, the power consumption (excluding that from reference supply) is 9 μW under supply voltage of 0.8 V, in which the analog portion consumes 5.4 μW, and the digital portion consumes 3.6 μW. The power consumption for each blocks from post layout simulation is shown in Figure 6.20. Please note 19% is for SAR and each sub-block is in clockwise order.

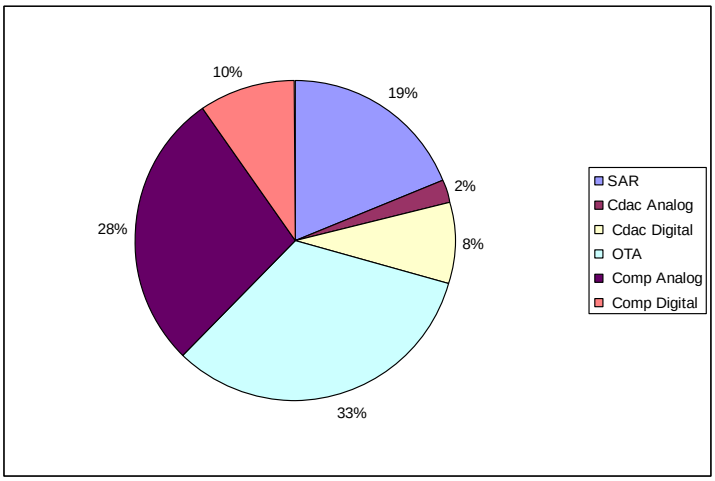

Figure 6.20: The power consumption for each sub-block.

With the calculated effective number-of-bits (*ENOB*) of 8.8, the figure-of-merit (*FOM*) is 20 fJ/conversion. Please notes FOM is defined as (not based on ERBW)

$$FOM = \frac{P}{F_s * 2^{ENOB}}, \qquad (6.10)$$

where, P is the power consumption, F_s is the conversion rate. This is because the targeted application is to convert DC signal from multiple input channels. The low power consumption is achieved by reducing the OTA's capacitive load during input tracking, by putting a small capacitor in series with the capacitor array. In addition, the OTA is reused as the pre-amplifier of the current-mode comparator. Low power digital circuits also contribute.

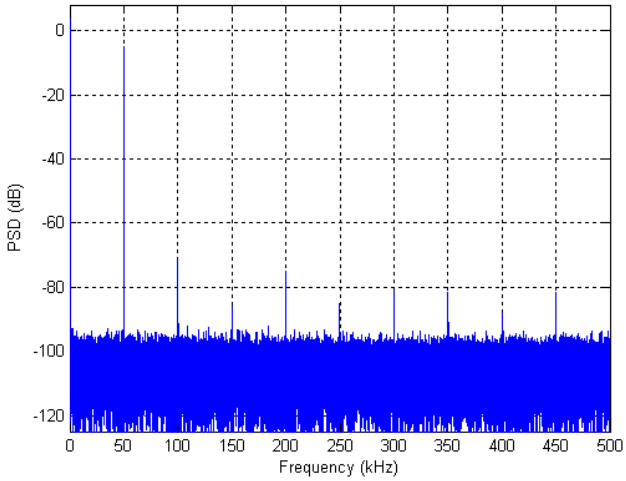

Figure 6.21: The measured FFT spectrum (131072 points).

The measured power consumption from V_{ref} is 3.2 μW, which is larger than required. This is expected after using polysilicon as C_{dac}'s shielding layer, which results in large parasitic capacitance from its bottom plate.

The experimental result is summarized in Table 6.2. The comparison with others' work is shown in Table 6.3.

Table 6.2: The summarized experimental results.

Items	Value
V_{DD}	0.8 V
V_{ref}	0.8V
V_{in} range	0 ~ 0.8 V
Clock	12 MHz
Conv. Rate	1 MS/s
Area	240 μm * 235 μm
Process	0.13 μm CMOS
DNL	-0.33/+0.56 LSB
INL	-0.61/+0.55 LSB
SNDR/SNR	55/56 dB
V_{ref} power	3.2 μW
V_{DD} power	9 μW
ENOB @DC	8.8 bits
FOM	20 fJ/conv.

Table 6.3: The performance comparison.

Items	[22]**, 2011**	[28]**, 2008**	[29]**, 2007**	**Work in Chap 5**	**This work**
Topology	Differential	Single-ended	Single-ended	Single-ended	Single-ended
Supply (V)	1.0	1.0	0.9	1.0	0.8
Process (μm)	0.09	0.18	0.18	0.13	0.13
Rate (MS/s)	10.24	0.1	0.2	1.0	1.0
Res. (bit)	8	12	8	10	10
DNL (LSB)	0.84	-2.00/+1.60	-0.90/+0.26	-0.31/+0.37	-0.33/+0.56
INL (LSB)	0.73	-2.50/+2.50	-0.53/+0.50	-0.30/+0.36	-0.61/+0.55
ENOB (bits)	7.77	9.4	7.58	9.0	8.8
Power (μW)	26	3.8	2.47	18.0	9.0
FOM(fJ/conv.) $FOM = \frac{P}{Fs * 2^{ENOB}}$	12	56	65	35	20
FOM(fJ/conv.) $FOM = \frac{P}{2 * ERBW * 2^{ENOB}}$	12	56	65	---	---

6.5 Conclusions

A low voltage, low power SAR ADC for sensing systems has been presented. To reduce the power consumption, a small capacitor is put in series with the capacitor array such that the capacitive load to amplifier during input tracking is lowered. In addition, the amplifier, which provides common mode during input tracking, is reused as the pre-amplifier for the current-mode latched comparator. In order to reduce the power consumption from the reference supply, a split capacitor array with dual thermometer decoders is also proposed.

CHAPTER 7 CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

In this thesis, four analog-to-digital converters have been presented, among which two are Delta-Sigma modulators and another two are successive approximation (SAR) ADCs. Although the design methodologies are very different between these two kinds of ADCs, they share the same target of this research work, which is to design ADCs with low power consumption even under low supply voltage.

For the Delta-Sigma modulators, the research target is to operate the Delta-Sigma modulator at high frequency under the constraints of low-voltage and low-power. The design novelties is on the combinations: reduced output swing by using input-feedforward topology; low OTA DC gain due to the suppressed gain non-linearity; simplified circuit design (for example, telescopic OTA) for design robustness at high frequency.

For the SAR ADCs, the research target is to increase their power efficiency, with the application target of bio-medical sensing systems, especially those with many input channels. The main design novelties are: using CMOS inverter as the OTA, assisted with an adaptive calibration scheme; reusing the V_{cm} buffer as the pre-amplifier for the current-mode latched comparator; dual thermometer decoders for the split capacitor array; serially connected capacitor array for smaller capacitive load to both ADC input and V_{cm} buffer.

7.2 Future Work

7.2.1 Delta Sigma Modulator

For the Delta-Sigma modulator, it is very difficult to invent a new topology. This can be proved by searching the literatures in the past 5 years. The focus is more on the implementation side, especially for a specific application. However, it is critical to get a good understanding of the pros and cons of different topologies.

One important observation is that the continuous-time Delta-Sigma modulator is more popular compared with the discrete-time one, especially within last 3 years. To my knowledge, the discrete-time modulators have been thoroughly explored in the 80s and 90s of last century. However, the potential applications of continuous-time modulator are not well discovered.

7.2.2 SAR ADC

For the proposed SAR ADC, there is still some room for further improvements. For the amplifier based on the CMOS inverter in the first SAR ADC, a better idea is shown in Figure 7.1, compared with that using the adaptive digital calibration technique.

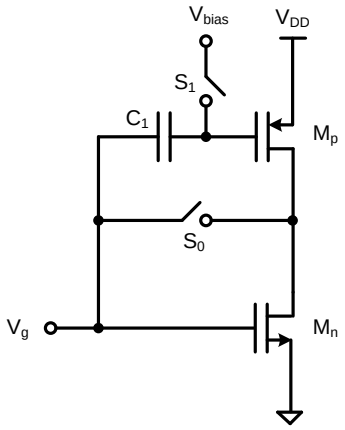

Figure 7.1: The proposed amplifier for future work in SAR ADC.

Before the input tracking period, both S_0 and S_1 are closed while the capacitors connected to the V_g node are floated. The capacitor C_1 records the potential difference between V_g and V_{bias}. After settled, the switch S_1 is opened to freeze the charge. Then, the amplifier works as same as a CMOS inverter with higher transconductance and slew rate, compared with the common-source amplifier used in the second SAR ADC, while the variations in transconductance due to process, supply and temperature are reduced.

To prevent the "short circuit" issue in the first SAR ADC while using CMOS inverter as the amplifier, a better solution is shown in Figure 7.2, with negative feedback as the key concept.

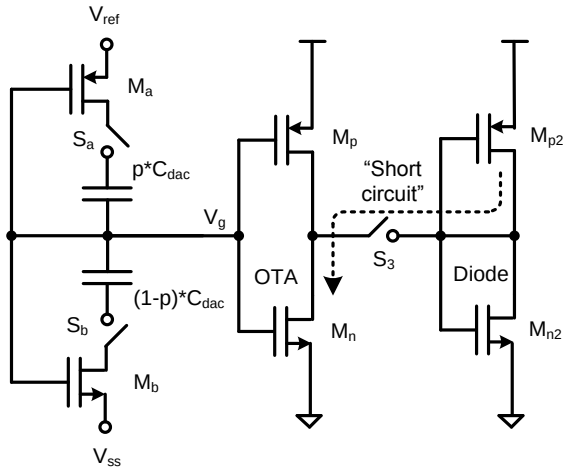

Figure 7.2: The proposed solution for "short circuit" issue.

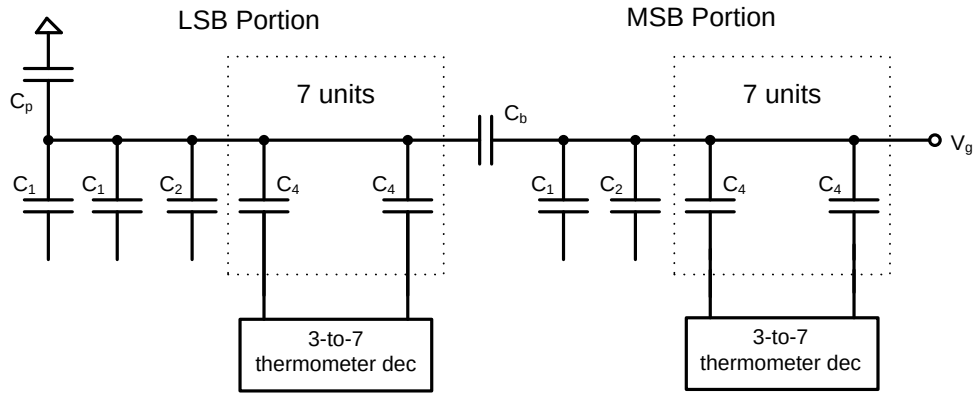

Figure 7.3: The modified split capacitor array, where $C_4=4C_1$, $C_2=2C_1$, $C_b=C_1$.

The proposed amplifier in Figure 7.1 can be combined with the serially-connected capacitor array in the second SAR ADC, in order to achieve higher power efficiency. In addition, with gain error being compensated, the split capacitor array can be simplified as shown in Figure 7.3. The single change is to use C_b=C_1 instead of 32/31*C_1 in conventional designs. This change only results in some gain error, which will be compensated. The benefit is easier layout of the capacitor array.

For the fabrication of the SAR ADC for future work, it is suggested to move away from the IBM 0.13 μm CMOS technology, which were adopted by two SAR ADCs in this work. For SAR ADC, capacitor array is the key design block. Both MIM and metal finger capacitor in this process are not favored due to process limitations.

7.2.3 SAR ADC in Biomedical Device

For the SAR ADC used in the biomedical devices, one possible improvement is to merge some ADC building blocks with the analog front-end, in order to save some power from the system level. One interesting application is the capacitive-coupled ECG device.

BIBLIOGRAPHY

[1] B. Murmann, "ADC performance survey 1997-2011," [Online]. Available: http://www.stanford.edu/~murmann/adcsurvey.html.

[2] H. Inose and Y. Yasuda, "A unity bit coding method by negative feedback," *IEEE Proceedings*, Vol. 51, pp. 1524-1535, Nov 1963.

[3] R. Schreier and G. C. Temes, "Understanding Delta-Sigma data converters", John Wiley & Sons, New York, 2004

[4] S. Hein and A. Zakhor, "On the stability of interpolative Sigma Delta modulators," *Proceedings of the 1991 IEEE International Symposium on Circuits and Systems*, vol. 3, pp. 1621-1624, June 1991.

[5] K. C. Chao, S. Nadeem, W. L. Lee, "A higher order topology for interpolative modulators for oversampling A/D converters", *IEEE Trans. Circuits Syst.*, vol. CAS-37, no. 3, pp. 309-318, March 1990

[6] T. Ritoniemi, T. Karema, and H. Tenhunen, "Design of stable high-order 1-bit sigma–delta modulators," *Proc. IEEE Int. Symp. Circuits and Systems*, pp. 3267–3270, May 1990.

[7] S. R. Norsworthy, R. Schreier, and G. C. Temes, "Delta-Sigma data converters, Theory, Design, and Simulation," IEEE Press, 1997.

[8] P. Balmelli, Q. Huang, "A 25 MS/s 14-b 200 mW Delta Sigma modulator in 0.18 µm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2161-2169, Dec. 2004.

[9] Ruoxin Jiang, Fiez, T.S., "A 14-bit delta-sigma ADC with 8× OSR and 4-MHz conversion bandwidth in a 0.18-µm CMOS process," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 63-74, Jan. 2004.

[10] R. Gaggl, M. Inversi, and A. Wiesbauer, "A power optimized 14-bit SC ΔΣ modulator for ADSL CO applications," *IEEE International Solid-State Circuits Conference*, vol.. 47, pp. 82-83, Feb. 2004.

[11] KiYoung Nam, Sang-Min Lee, Su, D.K., Wooley, B.A., "A low-voltage low-power sigma-delta modulator for broadband analog-to-digital conversion", *IEEE J. Solid-State Circuits*, vol. 40, no. 9, pp. 1855-1864, Sep. 2005.

[12] Brewer, R., Gorbold, J., Hurrell, P., Lyden, C., Maurino, R., Vickery, M., "A 100dB SNR 2.5MS/s output data rate ΔΣ ADC", *IEEE International Solid-State Circuits Conference*, pp. 172-591, Feb. 2005.

[13] Bosi, A., Panigada, A., Cesura, G., Castello, R., "An 80MHz 4× oversampled cascaded ΔΣ-pipelined ADC with 75dB DR and 87dB SFDR", *IEEE International Solid-State Circuits Conference*, pp. 174-591, Feb. 2005.

[14] Kwon, S., Maloberti, F., "A 14mW multi-bit Delta Sigma modulator with 82dB SNR and 86dB DR for ADSL2+ ", *IEEE International Solid-State Circuits Conference*, pp. 161-170, Feb. 2006.

[15] Y. Fujimoto, Y. Kanazawa, P. Lore, and M. Miyamoto, "An 80/10MS/s 76.3/7.01dB SNDR ΔΣ ADC for digital TV receivers;" *IEEE International Solid-State Circuits Conference*, pp. 76-77, Feb. 2006.

[16] Zhiheng Cao, Tongyu Song, Shouli Yan, "A 14 mW 2.5 MS/s 14 bit Delta Sigma modulator using split-path pseudo-differential amplifiers", *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2169-2179, Oct. 2007.

[17] Lee, K., Chae, J., Aniya, M., Hamashita, K., Takasuka, K., Takeuchi, S., Temes, G. C, "A noise-coupled time-interleaved Delta-Sigma ADC With 4.2 MHz bandwidth, -98 dB THD, and 79 dB SNDR", *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2601-2612, Dec. 2008.

[18] Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, Clifford Stein, "Introduction to algorithms", Second Edition, The MIT Press, 2009.

[19] J. L. McCreary and P. R. Gray, "All-MOS charge redistribution analog-to-digital conversion techniques. I.," *IEEE J. Solid-State Circuits*, vol. SC-10, no. 6, pp. 371-379, Dec. 1975.

[20] S. Yee, L. M. Terman, and L. G. Heller, "A two stage weighted capacitor network for D/A-A/D conversion," *IEEE J. Solid-State Circuits*, vol. SC-14, no. 4, pp. 778-781, Aug. 1979.

[21] Yip, M., A. Chandrakasan, "A resolution-reconfigurable 5-to-10b 0.4V-to-1V power scalable SAR ADC," *IEEE International Solid-State Circuits Conference*, pp. 190-191, Feb 2011.

[22] Harpe, P.J.A., Zhou, C., Yu Bi, van der Meijs, N.P., Xiaoyan Wang, Philips, K., Dolmans, G., de Groot, H., "A 26 μW 8 bit 10 MS/s asynchronous SAR ADC for low energy radios," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1585-1595, Jul. 2011.

[23] Sang-Hyun Cho, Chang-Kyo Lee, Jong-Kee Kwon, Seung-Tak Ryu, "A 550-μW 10-b 40-MS/s SAR ADC with multistep addition-only digital error correction," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1881-1892, Aug. 2011.

[24] van Elzakker, M., van Tuijl, E., Geraedts, P., Schinkel, D., Klumperink, E., Nauta, B., "A 10-bit charge-redistribution ADC consuming 1.9 μW at 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1007-1015, May 2010.

[25] Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Martins R.P., Maloberti F., "A 10-bit 100-MS/s reference-free SAR ADC in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1111-1121, Jun. 2010.

[26] Chun-Cheng Liu, Soon-Jyh Chang, Guan-Ying Huang, Ying-Zu Lin, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731-740, Apr. 2010.

[27] Yoshioka M., Ishikawa K., Takayama T., Tsukamoto S., "A 10b 50MS/s 820μW SAR ADC with on-chip digital calibration," *IEEE International Solid-State Circuits Conference*, pp. 384-385, Feb 2010.

[28] Agnes A., Bonizzoni E., Malcovati P., Maloberti F., "A 9.4-ENOB 1V 3.8μW 100kS/s SAR ADC with time-domain comparator," *IEEE International Solid-State Circuits Conference*, pp. 246-610, Feb. 2008.

[29] H.-C. Hong and G.-M. Lee, "A 65-fJ/conversion-step 0.9-V 200-kS/s rail-to-rail 8-bit successive approximation ADC," *IEEE J. Solid-State Circuits*, vol. 42, no. 10, pp. 2161–2168, Oct. 2007.

[30] Gambini S., Rabaey J., "Low-power successive approximation converter with 0.5 V supply in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2348-2356, Nov. 2007.

[31] Verma N., Chandrakasan A.P., "An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1196-1205, Jun. 2007.

[32] J. Silva, U. Moon, J. Steensgaard, and G. C. Temes, "A wideband low distortion Delta-Sigma ADC topology," *IEEE Electronics Letters*, vol. 37, pp. 737–738, June 2001.

[33] A. Gharbiya, D.A. Johns, "A 12-bit 3.125 MHz bandwidth 0–3 MASH Delta-Sigma modulator", *IEEE Journal of Solid-State Circuits*, vol. 44, Issue 7, Jul 2009.

[34] Y. Fujimoto, Y. Kanazawa, P.L. Re, K., Iizuka, "A 100 MS/s 4 MHz bandwidth 70 dB SNR Delta Sigma ADC in 90 nm CMOS", *IEEE Journal of Solid-State Circuits*, Volume 44, Issue 6, Jun 2009.

[35] A. Gharbiya, D.A. Johns, "On the implementation of input-feedforward delta-sigma modulators," *IEEE Trans. Circuits Syst. II*, Express Briefs, vol.53, no.6, pp.453–457, June 2006.

[36] L. Yao, M. Steyaert and W. Sansen, "A 1-V, 1-MS/s, 88-dB Sigma-Delta modulator in 0.13-μm digital CMOS technology," *Digest of Technical Papers IEEE Symposium on VLSI circuits*, June 2005.

[37] A. Marques, V. Peluso, M. Steyaert, and W. Sansen, "Optimal parameters for Delta-Sigma modulator topologies," *IEEE Trans. Circuits Syst*., vol. 45, no. 9, pp. 1232–1241, Sept. 1998.

[38] O.Choksi and L.R Carley, "Analysis of switched-capacitor common-mode feedback circuit," *IEEE Trans. Circuits and Systems II*, vol.50, no.12, pp. 906-917, Dec 2003.

[39] T. C. Choi, R. T. Kaneshiro, R. W. Brodersen, P. R. Gray, W. B. Jett, and M. Wilcox, "High-frequency CMOS switched-capacitor filters for communications application," *IEEE J. Solid-State Circuits*, vol. 18, pp. 652 – 664, Dec. 1983.

[40] M. Abo, "Design for reliability of low-voltage, switched-capacitor circuits," Ph.D. dissertation, California Inst. of Technol., 1999.

[41] P. Balmelli, "Broadband sigma-delta A/D converters," Ph.D. dissertation, Swiss Federal Institute of Technology, Zurich, Switzerland, 2003.

[42] M. S. Peng and H.-S. Lee, "Study of substrate noise and techniques for minimization," in *Symp. VLSI Circuits Dig. Tech*. Papers, Jun. 2003, pp. 197–200.

[43] M. Ingels and M. Steyaert, "Design strategies and decoupling techniques for reducing the effects of electrical interference in mixed-mode IC's", *IEEE J. Solid-State Circuits*, vol. 32, Jul. 1997.

[44] R. Reutemann, P. Balmelli, and Q. Huang, "A 33 mW 14b 2.5 MS/s Delta-Sigma A/D converter in 0.25-um digital CMOS," *IEEE International Solid-State Circuits Conference*, pp. 316–317, Feb. 2002.

[45] P. Spruyt and S. Schelstraete, "VDSL, from concept to chips," in *Proc. 26th ESSCIRC*, Stockholm, Sweden, pp. 30–37, Sep. 2000.

[46] E. J. van der Zwan and E. C. Dijkmans, "A 0.2-mW CMOS Delta-Sigma modulator for speech coding with 80 dB dynamic range," *IEEE J. Solid-State Circuits*, vol. 31, pp. 1873–1880, Dec. 1996.

[47] R. Schreier, The Sigma-Delta Toolbox, Delsig Matlab Toolbox, Version 5.1 ed., 1998.

[48] J. G. Kenney and L. R. Carley, "Design of multibit noise-shaping data converters," *Analog Integrated Circuits Signal Processing Journal*, vol. 3, pp. 259-272, 1993

[49] S. Gambini and J. Rabaey, "Low-power successive approximation converter with 0.5 V supply in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2348-2356, Nov. 2007.

[50] M. Elzakker, E. Tuijl, P. Geraedts, D. Schinekel, E. Klumperink, and B. Nauta, "A 1.9 uW 4.4 fJ/conversion-step 10b 1 MS/s charge-redistribution ADC," *IEEE International Solid-State Circuits Conference*, pp. 244–246, Feb. 2008.

[51] G. Promitzer, "12-bit low-power fully differential switched capacitor non-calibrating successive approximation ADC with 1 MS/s," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1138–1143, Jul. 2001.

[52] N. Verma and A. P. Chandrakasan, "An ultra low energy 12-bit rate-resolution scalable SAR ADC for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1196-1205, Jun. 2007.

[53] M. Yip and A.P. Chandrakasan, "A resolution-reconfigurable 5-to-10b 0.4V-to-1V power scalable SAR ADC," *IEEE International Solid-State Circuits Conference*, Feb 2011.

[54] S. Mortezapour and E.K.F. Lee, "A 1-V, 8-Bit successive approximation ADC in standard CMOS process," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 642-646, Apr. 2000.

[55] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultralow-energy ADC for smart dust," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1123–1129, Jul. 2003.

[56] A. Nikoozadeh and B. Murmann, "An analysis of latch comparator offset due to load capacitor mismatch," *IEEE Trans. Circuits Syst. II*, Exp. Briefs, vol. 53, no. 12, pp. 1398–1402, Dec. 2006.

[57] Y. S. Yee, L. M. Terman, and L. G. Heller, "A two stage weighted capacitor network for D/A-A/D conversion," *IEEE J. Solid-State Circuits*, vol. SC-14, no. 4, pp. 778-781, Aug. 1979.

[58] Brian P. Ginsburg, Anantha P. Chandrakasan, "An energy-efficient charge recycling approach for a SAR converter with capacitive DAC," *IEEE Symposium on Circuits and Systems*, pp. 184-187, May 2005.

[59] G. Yin, F. Eynde, and W. Sansen, “A high-speed CMOS comparator with 8-b resolution,” *IEEE J. Solid-State Circuits*, vol. 27, pp. 208–211, Dec. 1990.

[60] G. Wegmann, E. A. Vittoz, and F. Rahali, “Charge injection in analog MOS switches,” *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 1091–1097, Dec. 1987.